

High Temperature Configurable Logic Gates

Preliminary Datasheet

Version: 1.1
(see note 1)

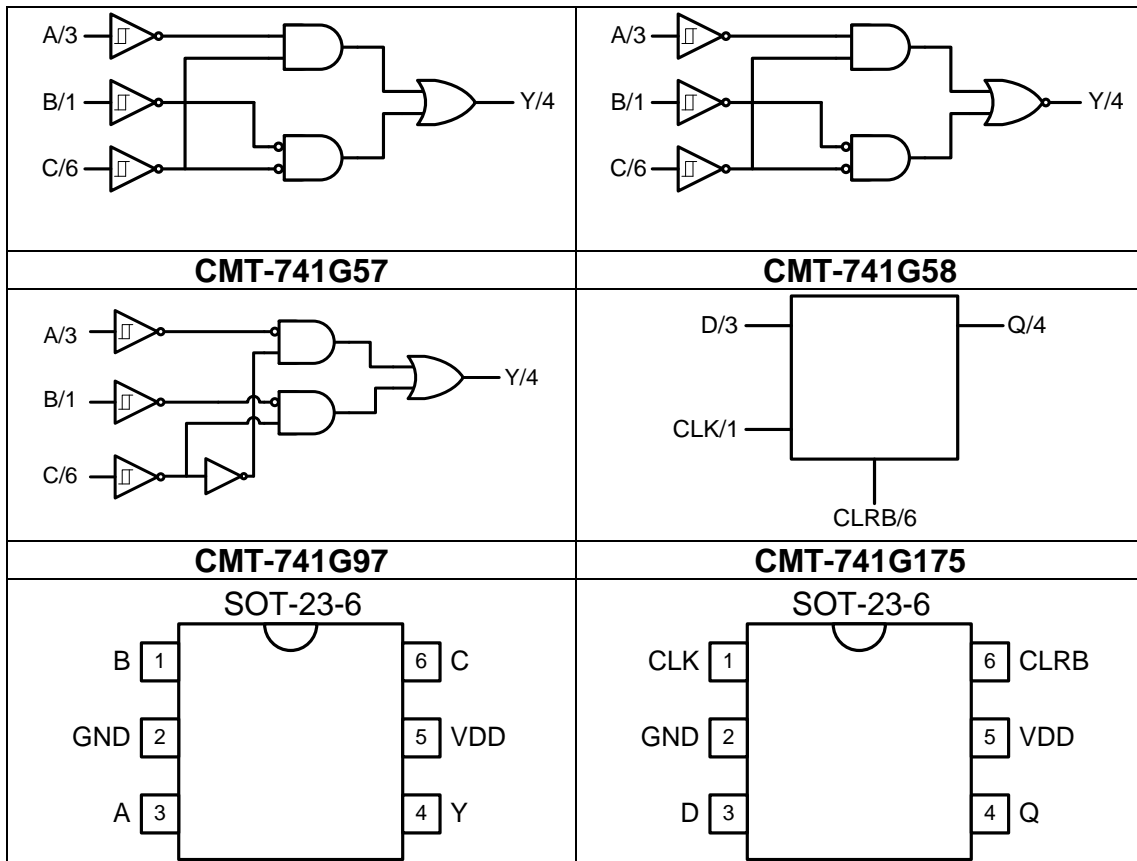
General description

The CMT-741Gxx are 4 high temperature configurable devices enabling 13 different logic functions: INV, BUFFER, AND, AND w/ inverted input, NAND, NAND w/ inverted input, OR, NOR, NOR w/ inverted input, XOR, NXOR, MUX and D Flip-Flop.

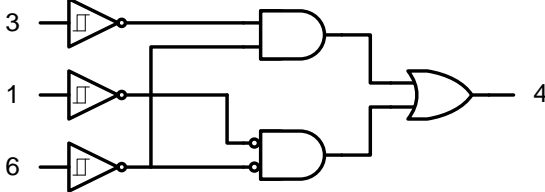
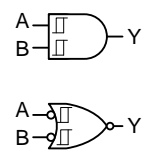
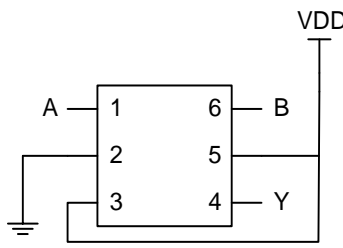
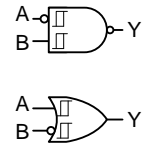
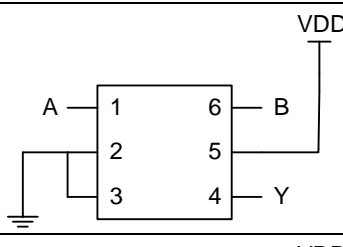
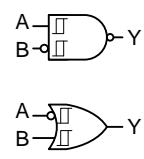
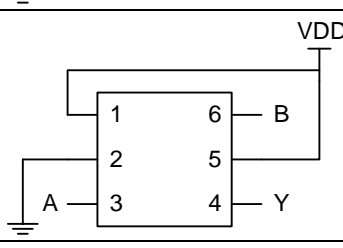
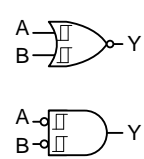
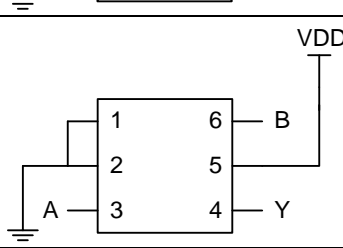
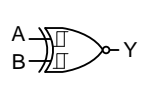
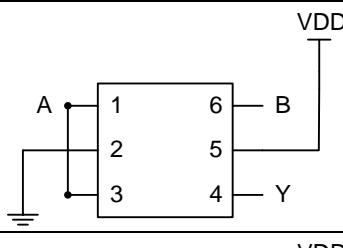
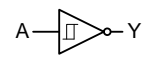
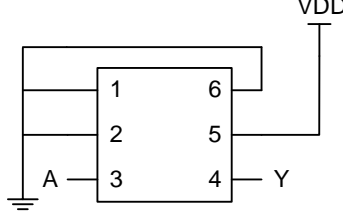
These devices are optimized for high-end industrial applications and specified for operating junction temperature from -55°C up to +175°C (Tj).

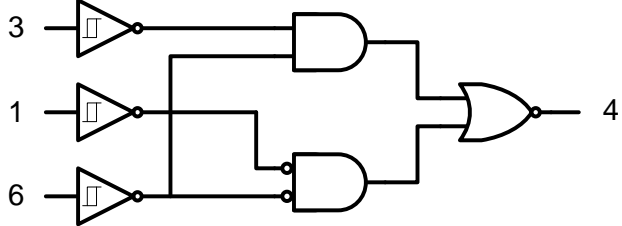
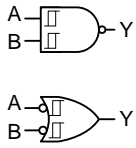
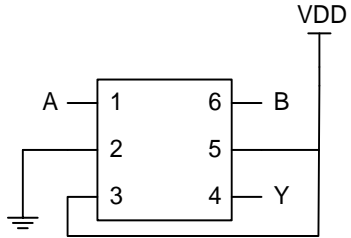
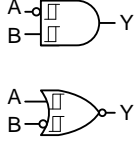
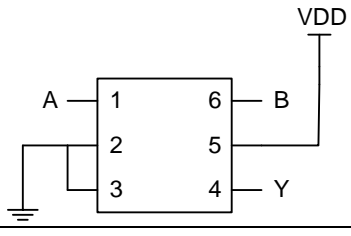
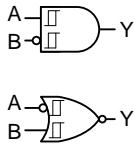
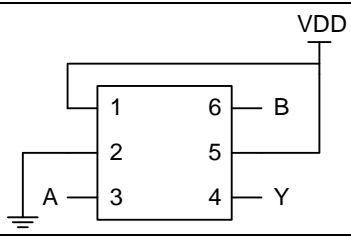
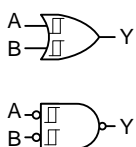
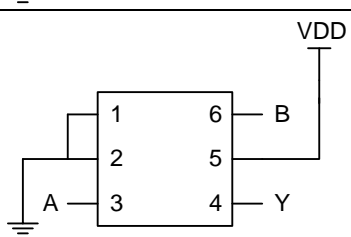
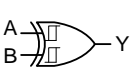
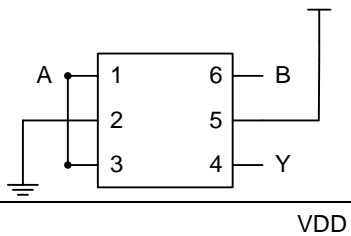
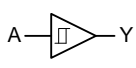
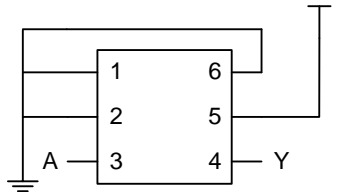
Features

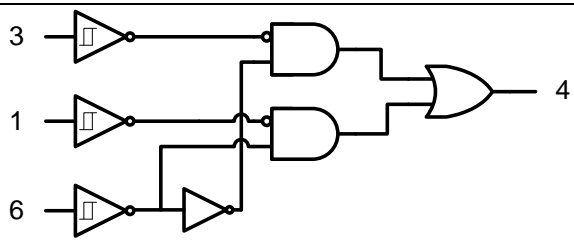
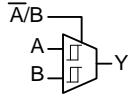
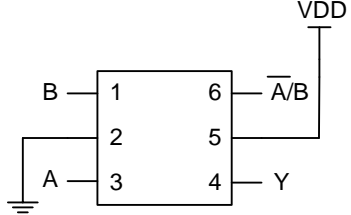
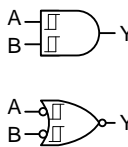
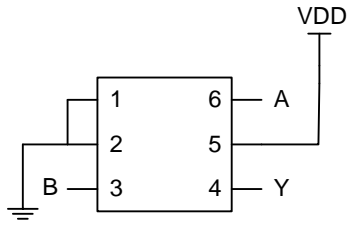
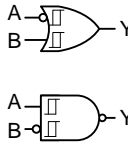
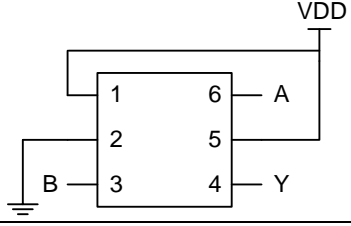
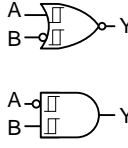
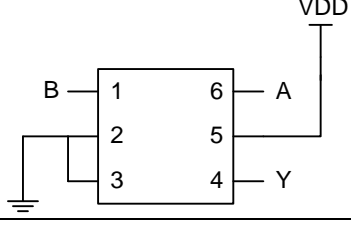
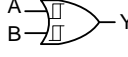
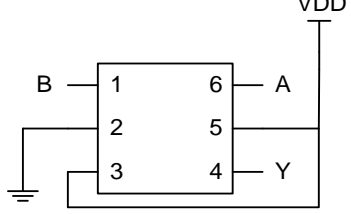
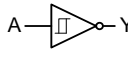
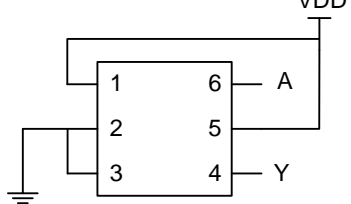
- Operating junction temperature: from -55°C to +175°C (Tj)
- Supply voltage: 1.65V to 5.5V
- Inputs can be driven by 3.3V or 5V signals, even for lower supply voltage
- Schmitt trigger inputs for high immunity to slow changing signals
- ± 16 mA output drive current
- CMOS low power consumption
- ESD: 2000V HBM or 200V MM
- Lead Free Finish & RoHS compliant
- Tiny package: SOT-23 6 leads



Note 1 Please always refer to the latest datasheet version available at <http://www.cissoid.com/files/files/products/galaxy/CMT-741GXX.pdf>

Logic configurations		
CMT-741G57		
		
Configuration 1 2-Input AND Gate 2-Input NOR Gate with Both Inputs Inverted		
Configuration 2 2-Input NAND Gate with A Input Inverted 2-Input OR Gate with B Input Inverted		
Configuration 3 2-Input NAND Gate with B Input Inverted 2-Input OR Gate with A Input Inverted		
Configuration 4 2-Input NOR Gate 2-Input AND Gate with Both Inputs Inverted		
Configuration 5 2-Input XNOR Gate		
Configuration 6 Inverter		

Logic configurations		
CMT-741G58		
		
Configuration 1 2-Input NAND Gate 2-Input OR Gate with Both Inputs Inverted		
Configuration 2 2-Input AND Gate with A Input Inverted 2-Input NOR Gate with B Input Inverted		
Configuration 3 2-Input AND Gate with B Input Inverted 2-Input NOR Gate with A Input Inverted		
Configuration 4 2-Input OR Gate 2-Input NAND Gate with Both Inputs Inverted		
Configuration 5 2-Input XOR Gate		
Configuration 6 Buffer		

Logic configurations CMT-741G97		
		
Configuration 1 2 to 1 Multiplexer		
Configuration 2 2-Input AND Gate 2-Input NOR Gate with Both Inputs Inverted		
Configuration 3 2-Input OR Gate with A Input Inverted 2-Input NAND Gate with B Input Inverted		
Configuration 4 2-Input NOR Gate with B Input Inverted 2-Input AND Gate with A Input Inverted		
Configuration 5 2-Input OR Gate		
Configuration 6 Inverter		

CMT-741G57/CMT-741G58/CMT-741G97/CMT-741G175
Absolute Maximum Ratings(see note 2)

Symbol	Parameter	Min.	Max.	Units
V _{DD}	Supply Voltage Range	-0.5	6.5	V
V _I	Input Voltage Range	-0.5	6.5	V
V _O	Voltage applied to output in high or low state	-0.3	Min(V _{DD} +0.5, 6.5V)	V
I _{IK}	Input Clamp Current (V _I <0)		-30	mA
I _{OK}	Output Clamp Current (V _O <0 V _O >V _{DD})		30	mA
I _O	Continuous Output Current		20	mA
T _J	Operating Junction Temperature	-55	175	°C
T _{STG}	Storage Temperature	-55	175	°C
ESD HBM	ESD Rating (Human Body Model)	2		kV
ESD MM	ESD Rating (Machine Model)	200		V

Operating conditions

Symbol	Parameter	Min.	Max.	Units
V _{DD}	Supply Voltage Range	-0.5	5.5	V
V _I	Input Voltage Range	-0.5	5.4	V
V _O	Voltage applied to output in high or low state	-0.3	Min(V _{DD} +0.5, 5.5V)	V
I _{OH}	High-Level Output Current	V _{DD} =1.65V	4	mA
		V _{DD} =2.3V	8	
		V _{DD} =3V	12	
		V _{DD} =4.5V	16	
I _{OL}	Low-Level Output Current	V _{DD} =1.65V	4	mA
		V _{DD} =2.3V	8	
		V _{DD} =3V	12	
		V _{DD} =4.5V	16	
Δt/ΔV _I	Input transition rise or fall time	V _{DD} =1.8V±10%	20	ns/V
		V _{DD} =2.5V±10%	20	
		V _{DD} =3.3V±10%	10	
		V _{DD} =5V±10%	5	
T _J	Operating Junction Temperature	-55	175	°C
T _A	Operating Ambient Temperature	-55	175	°C

Electrical Characteristics

Symbol	Parameter	Test conditions	V _{DD}	Min.	Typ	Max.	Units
CI			3.3		2.7		pF
C _{PD}	Power dissipation capacitance	F= 10 MHz	1.8 to 5V		7.43		pF
Θ _{JA}	Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout				204		°C/W
Θ _{JC}					52		°C/W

Note 2 : Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

**CMT-741G57/CMT-741G58/CMT-741G97/CMT-741G175
Electrical Characteristics**

Bold underlined values indicate values over the whole temperature range ($-55^{\circ}\text{C} < T_J < +175^{\circ}\text{C}$); All typical values are at $T_A=25^{\circ}\text{C}$

Symbol	Parameter	Test conditions	V _{DD}	Min.	Typ	Max.	Units
V _{T+}	Positive-going Input Threshold Voltage		1.8V	<u>1.06</u>		<u>1.26</u>	V
			2.5V	<u>1.47</u>		<u>1.68</u>	
			3.3V	<u>1.9</u>		<u>2.13</u>	
			5V	<u>2.78</u>		<u>3.04</u>	
V _{T-}	Negative-going Input Threshold Voltage		1.8V	<u>0.57</u>		<u>0.74</u>	V
			2.5V	<u>0.86</u>		<u>1.01</u>	
			3.3V	<u>1.13</u>		<u>1.35</u>	
			5V	<u>1.68</u>		<u>2.05</u>	
ΔV _T	Hysteresis (V _{T+} - V _{T-})		1.8V	<u>0.44</u>		<u>0.53</u>	V
			2.5V	<u>0.58</u>		<u>0.69</u>	
			3.3V	<u>0.71</u>		<u>0.84</u>	
			5V	<u>0.97</u>		<u>1.18</u>	
V _{OH}	High Level Output voltage	I _{OH} =4mA	1.65V	<u>1.26</u>			V
		I _{OH} =8mA	2.3V	<u>1.81</u>			
		I _{OH} =12mA	3V	<u>2.46</u>			
		I _{OH} =16mA	4.5V	<u>4.01</u>			
V _{OL}	Low Level Output voltage	I _{OH} =4mA	1.65V			<u>0.24</u>	V
		I _{OH} =8mA	2.3V			<u>0.31</u>	
		I _{OH} =12mA	3V			<u>0.36</u>	
		I _{OH} =16mA	4.5V			<u>0.35</u>	
I _{IN}	Input Current	V _I =5V or V _{SS}	1.65V to 5.5V			<u>6</u>	μA
I _{DD}	Supply Current	V _I =5V or V _{SS} I _O =0	1.65V to 5.5V			<u>8</u>	μA

**CMT-741G57/CMT-741G58/CMT-741G97
Timing Characteristics**

Bold underlined values indicate values over the whole temperature range ($-55^{\circ}\text{C} < T_J < +175^{\circ}\text{C}$); All typical values are at $T_A=25^{\circ}\text{C}$

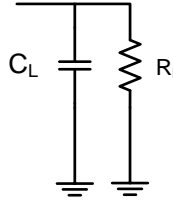
Symbol	Parameter	Test conditions	V _{DD}	Min.	Typ	Max.	Units
t _{PD}	Propagation delay from any input to output	CL=30pF RL=1KΩ	1.65V - 1.95V		12.7	<u>26.6</u>	ns
		CL=30pF RL=500Ω	2.25V - 2.75V		7.68	<u>15.7</u>	
		CL=50pF RL=500Ω	3V - 3.6V		6.38	<u>12.7</u>	
		CL=50pF RL=500Ω	4.5V - 5.5V		4.78	<u>8.8</u>	

CMT-741G175
Timing Characteristics

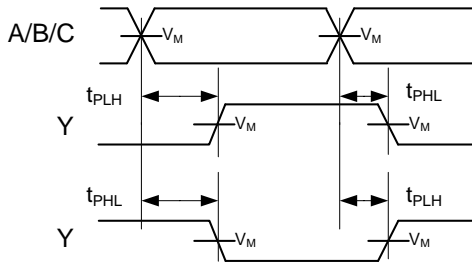
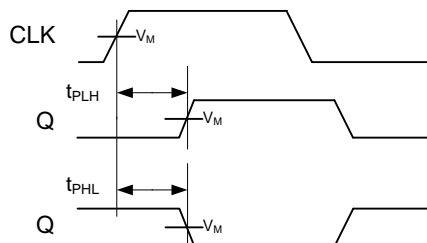
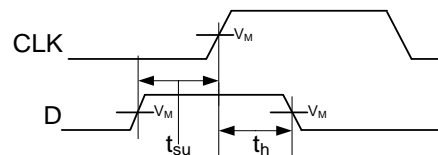
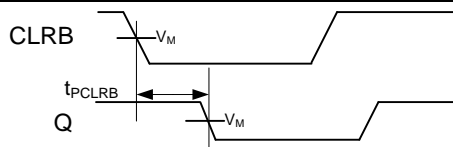
Bold underlined values indicate values over the whole temperature range ($-55^{\circ}\text{C} < T_J < +175^{\circ}\text{C}$); All typical values are at $T_A=25^{\circ}\text{C}$

Symbol	Parameter	Test conditions	V _{DD}	Min.	Typ	Max.	Units
f _{MAX}	Maximum Frequency	CL=30pF RL=1KΩ	1.65V - 1.95V	<u>20</u>			MHz
		CL=30pF RL=500Ω	2.25V - 2.75V	<u>35</u>			
		CL=50pF RL=500Ω	3V - 3.6V	<u>50</u>			
		CL=50pF RL=500Ω	4.5V - 5.5V	<u>70</u>			
t _{WCLK}	CLK Minimum Pulse Width		1.65V - 1.95V	<u>2</u>			ns
			2.25V - 2.75V	<u>2</u>			
			3V - 3.6V	<u>2</u>			
			4.5V - 5.5V	<u>1</u>			
t _{WCLRB}	CLRB Minimum Pulse Width		1.65V - 1.95V	<u>3</u>			ns
			2.25V - 2.75V	<u>2</u>			
			3V - 3.6V	<u>2</u>			
			4.5V - 5.5V	<u>2</u>			
t _{PD}	Propagation delay from CLK positive edge to output	CL=30pF RL=1KΩ	1.65V - 1.95V			<u>27.43</u>	ns
		CL=30pF RL=500Ω	2.25V - 2.75V			<u>16</u>	
		CL=50pF RL=500Ω	3V - 3.6V			<u>12.98</u>	
		CL=50pF RL=500Ω	4.5V - 5.5V			<u>8.96</u>	
t _{PCLRB}	Propagation delay from CLRB negative edge to output	CL=30pF RL=1KΩ	1.65V - 1.95V			<u>24.33</u>	ns
		CL=30pF RL=500Ω	2.25V - 2.75V			<u>13.65</u>	
		CL=50pF RL=500Ω	3V - 3.6V			<u>10.91</u>	
		CL=50pF RL=500Ω	4.5V - 5.5V			<u>7.8</u>	
t _{SU}	Setup time		1.65V - 1.95V	<u>2</u>			ns
			2.25V - 2.75V	<u>1</u>			
			3V - 3.6V	<u>1</u>			
			4.5V - 5.5V	<u>1</u>			
t _H	Hold time		1.65V - 1.95V	<u>1</u>			ns
			2.25V - 2.75V	<u>1</u>			
			3V - 3.6V	<u>1</u>			
			4.5V - 5.5V	<u>1</u>			

Parameter Measurement Information (notes3,4)

 From Output
 Under Test


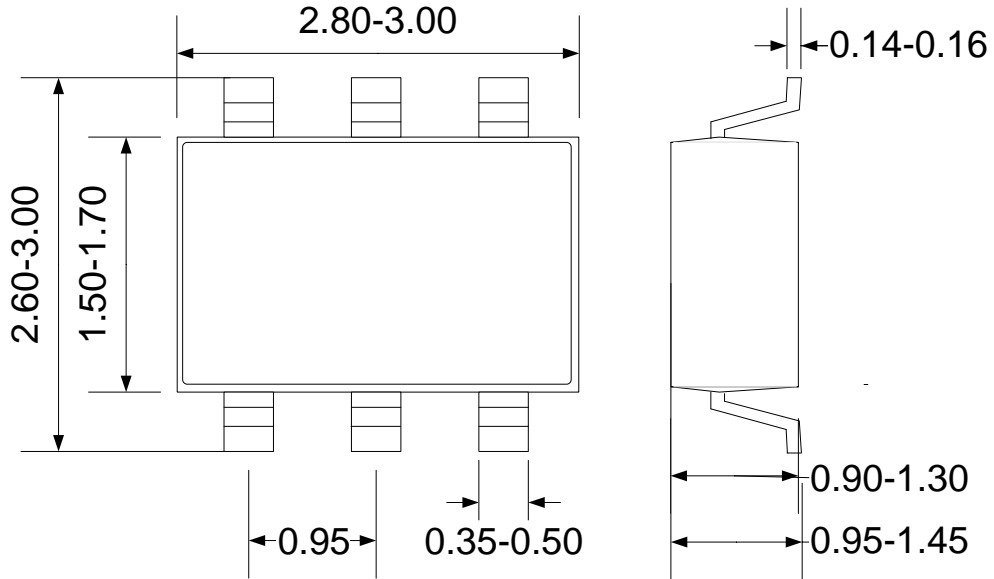
V_{DD}	Inputs		V_M	C_L	R_L
	V_I	t_r/t_f			
$1.8V \pm 0.15V$	V_{DD}	$\leq 2ns$	$V_{DD}/2$	30pF	1000 Ω
$2.5V \pm 0.2V$				30pF	500 Ω
$3.3V \pm 0.3V$				50pF	500 Ω
$5V \pm 0.5V$				50pF	500 Ω

CMT-741G57/CMT-741G58/CMT-741G97

Voltage Waveform
Propagation Delay times
Inverting and Non Inverting Outputs
CMT-741G175

Voltage Waveform
Propagation Delay times wrt CLK

Voltage Waveform
Set-up and Hold times wrt CLK

Voltage Waveform
Propagation Delay times wrt CLRB

 Note 3 C_L load capacitance includes PCB and probe capacitance

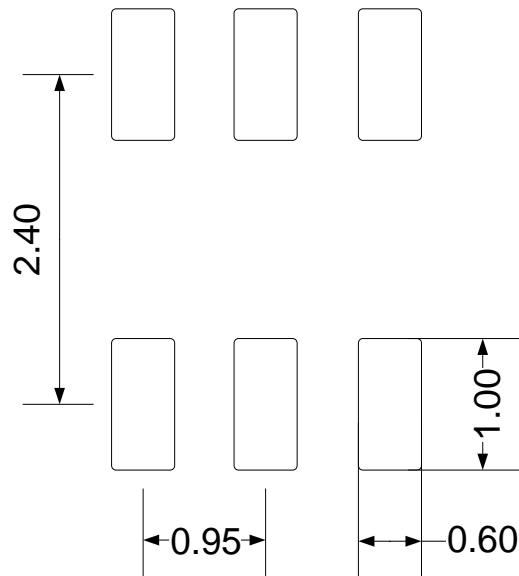
 Note 4 : t_{PHL} and t_{PLH} are the same as t_{PD}

Package Drawing



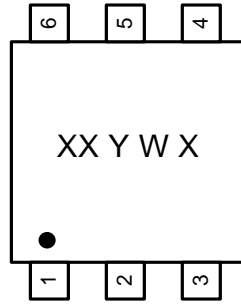
Physical dimensions in mm (tolerance : +/- 0.2 mm)

Suggested Pad Layout



Physical dimensions in mm (tolerance : +/- 0.2 mm)

Marking information



XX	Product identification code
Y	Year: [0-9]
W	Week: A-Z: [1-29], a-z: [27-52], z=52 and 53
X	Internal code

Ordering Information

Product Name	Ordering Reference	Package	Marking
CMT-741G57	CMT-741G57A-SOT-23-6	SOT-23-6	AA
CMT-741G58	CMT-741G58A-SOT-23-6	SOT-23-6	AC
CMT-741G97	CMT-741G97A-SOT-23-6	SOT-23-6	AB
CMT-741G175	CMT-741G175A-SOT-23-6	SOT-23-6	AD

Contact & Ordering

CISSOID S.A.

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