CISSOID
POWER SEMICONDUCTORS

3-Phase 1200V/450A SiC MOSFET Intelligent Power Module CXT-PLA3SA12450A-Preliminary Datasheet

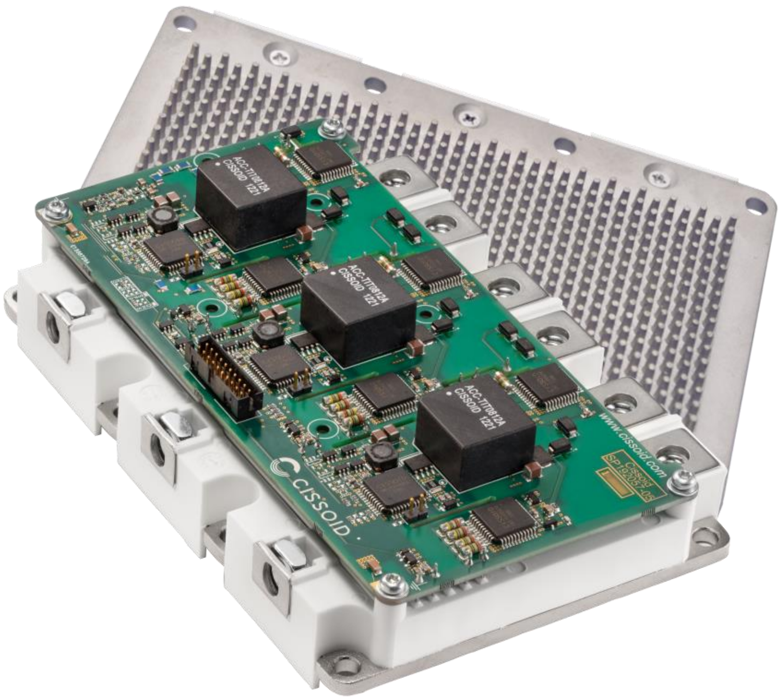
Version: 1.13
6-Sep-24
(Last Modification Date)

General description

CXT-PLA3SA12450A is a 3-phase 1200V/450A SiC MOSFET Intelligent Power Module integrating the power switches and the gate driver based on CISSOID HADES2® chipset.

With its **pin fin baseplate**, this module addresses high power density water cooled converters offering a SiC power module designed for operation at high junction temperature (up to 175°C). This solution gives access to the full benefits of SiC technology to achieve high power density thanks to low switching losses and high temperature operation.

The integration of the gate driver together with the power module give direct access to a fully validated and optimized solution in terms of switching speed and losses, robustness againt dI/dt and dV/dt and protection of the power stages (Desat, UVLO, AMC, SSD).



Key Features

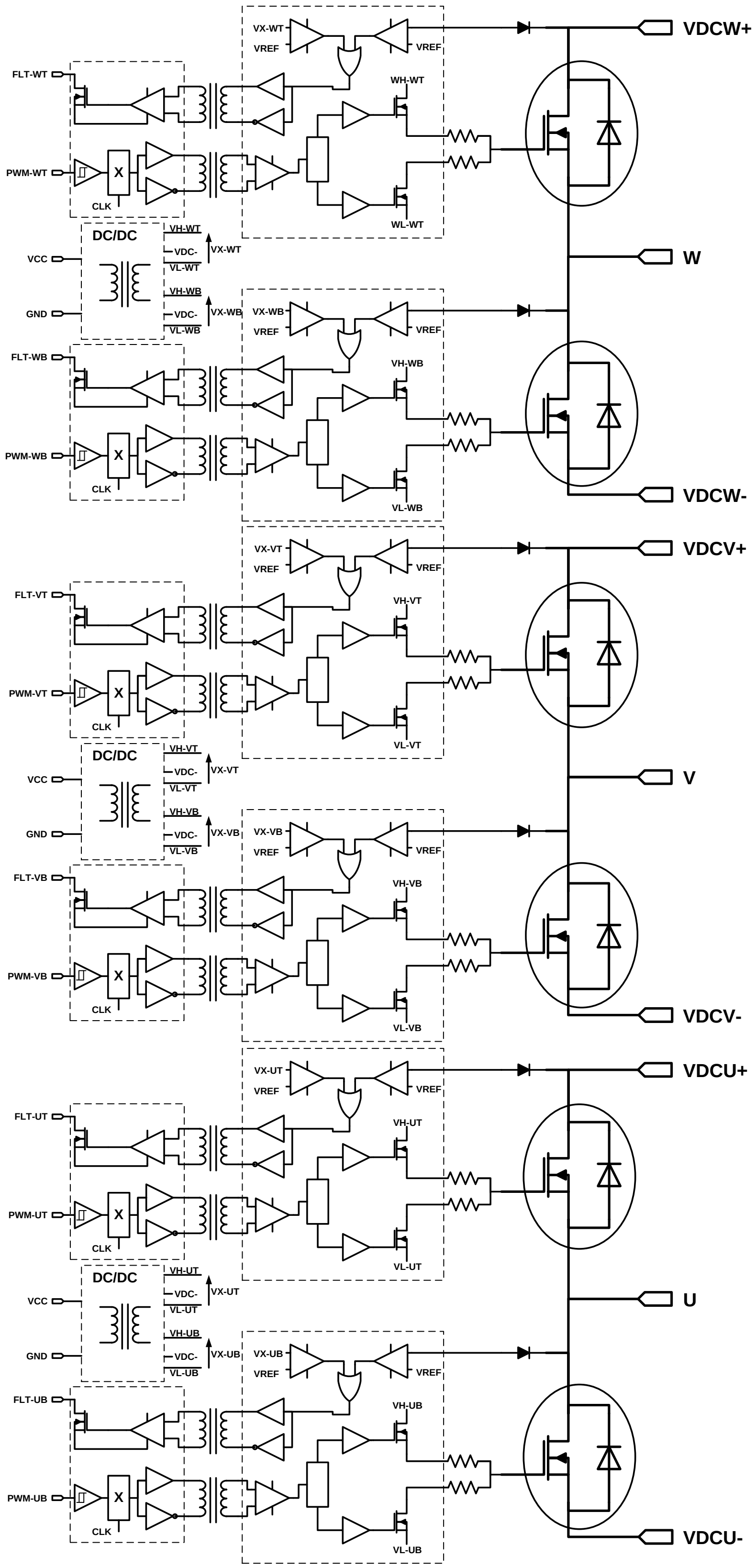
- VDS breakdown voltage: 1200V
- Low R_{DSON}[1]: typ 3.25mΩ
- Max Continuous current:
  - 450A typ. @ Tc=25°C
  - 350A typ. @ Tc=90°C
- Thermal resistance (J2C):
  - 0.13 °C/W typ.
- Max 175°C operating junction temperature (power devices)
- Switching Energy@ 600V/300A:
  - Eon: 8.42 mJ
  - Eoff: 7.05 mJ
- Switching frequency: 50kHz Max [2]
- Isolation (baseplate – power pins):
  - 5000VDC (1min)
- Common mode transient immunity:
  - >50kV/µs
- Dimensions:
  - 104(W) x 154(L) X 34(H) (all in mm)
- Weight: 590g
- Single power supply (VCC):
  - +12V to +18V
- Max 125°C operating ambient temperature (gate driver)
- Isolation (primary – secondary):
  - 3000VDC (1min)
- Parasitic capacitance:
  - typ 11pF per phase
- PWM input signal
  - 5V Schmitt trigger input
  - Active-High (Active-Low as an option)
- Open-drain fault reporting:
  - per side (top or bottom)
  - per phase as an option
- Turn-On/Off delay: 180ns typ.
- Under voltage lockout (UVLO)
  - On VCC
  - On internally generated secondary supplies
- Desaturation protection
- Soft Shutdown turn-off (SSD)
- Negative gate drive (-3V)
- Active Miller Clamping (AMC)
- Gate-Source Short-circuit Protection

Ordering Information

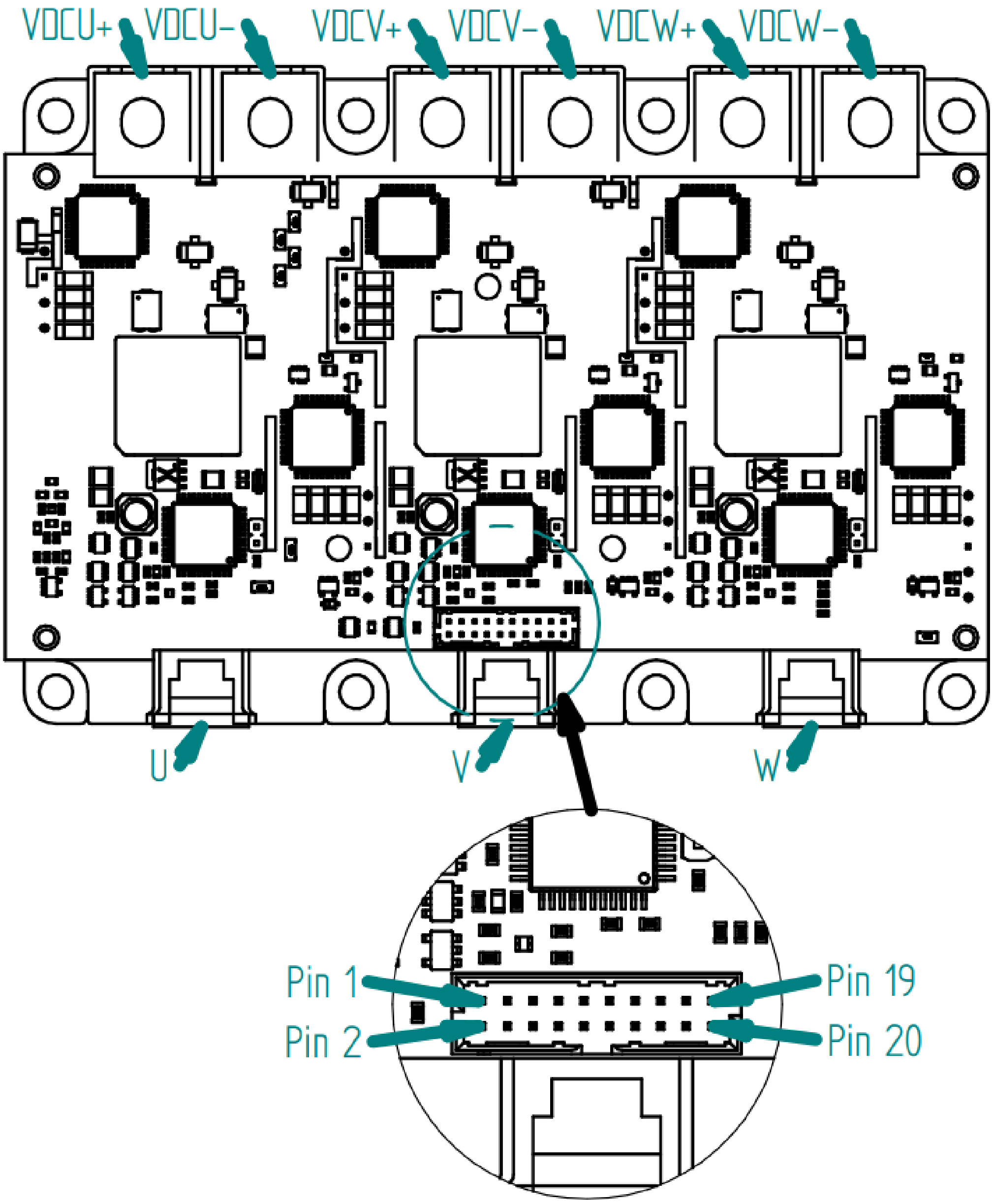
Product Name	Ordering Reference	Marking
CXT-PLA3SA12450A	CXT-PLA3SA12450AA	CXT-PLA3SA12450AA

[1] Package resistance excluded
[2] With Gate driver temperature derating from 25KHz to 50KHz (see curve at page 17)

Block diagram



Pinout[3]



[3] "VDCU+, VDCV+, VDCW+", "VDCU-, VDCV-, VDCW-" are not connected to each other internally

Pinout (cnt'd)

Interface	Pin	Pin name	Description
POWER		**VDCU+**	U Phase positive power supply
		VDCU-	U Phase negative power supply
		VDCV+	V Phase positive power supply
		VDCV-	V Phase negative power supply
		VDCW+	W Phase positive power supply
		VDCW-	W Phase negative power supply
		U	Half-Bridge output U
		V	Half-Bridge output V
		W	Half-Bridge output W

CONTROL	**Pin 1**	**PWM-UT**	PWM input high-side phase U
	Pin 2	**PWM-UB**	PWM input low-side phase U
	Pin 3	**TEMP-U**	Phase U temperature measurement output
	Pin 4	**RSTN**	Reset signal (active low); while low, forces all PWM to inactive state
	Pin 5	**PWM-VT**	PWM input high-side phase V
	Pin 6	**VDCM**	DC BUS voltage monitoring output
	Pin 7	**PWM-VB**	PWM input low-side phase V
	Pin 8	**GND**	Gate driver negative power supply
	Pin 9	**FLT-T-V**	Phase V fault output or 3 phase high-side (=top) fault output
	Pin 10	**GND**	Gate driver negative power supply
	Pin 11	**FLT-B-U**	Phase U fault output or 3 phase low-side (=bottom) fault output
	Pin 12	**VCC**	Gate driver positive power supply
	Pin 13	**TEMP-V**	Phase V temperature measurement output
	Pin 14	**VCC**	Gate driver positive power supply
	Pin 15		
	Pin 16	**GND**	Gate driver negative power supply
	Pin 17	**FLT-W**	Phase W fault output (not used in case of fault reporting per side)
	Pin 18	**TEMP-W**	Phase W temperature measurement output
	Pin 19	**PWM-WT**	PWM input high-side phase W
	Pin 20	**PWM-WB**	PWM input low-side phase W

Max Absolute Ratings

Parameter	Symbol	Condition	Value	Unit
Case temperature	T_C		-40°C to 150°C	°C
Storage temperature	T_{STG}		-40°C to 125°C	°C
Weight	g		590	g

"SiC MOSFET Power module"

Parameter	Symbol	Condition	Value	Unit
Drain – Source Voltage	V_{DS}	T_j=25°C	1200	V
		T_j=175°C	1200	V
MOSFET Continuous Drain Current	I_D	V_{GS} =15V, T_C=25°C, Tj<175°C	450	A
		V_{GS} =15V,T_C=90°C, Tj<175°C	350	A
Pulsed Drain Current	I_{Dpulse}	pulse width t_p limited by T_{jmax}	720	A
Junction temperature	Tj		175°C	°C
Case and Storage temperatures	T_C,T_{STG}		-40°C to 150°C	°C
Stray Inductance	L_{Stray}	Between VDCX+ and VDCX-	11.2	nH
Package resistance @ 25°C[4]		Between VDCX+ and phase output	0.7	mΩ
		Between VDCX- and phase output	0.7	mΩ
Clearance distance		From VDCX+ to VDCX-	5.6	mm
		From U,V,W to Baseplate	12	mm
		From VDCX+,VDCX- to Baseplate	12.5	mm
		From Gate driver HS,LS to Primary	2.55	mm
		From Gate driver Primary to U,V,W	7.63	mm
		From Gate driver HS,LS to VDCX+,VDCX-	5	mm
Creepage distance		From VDCX+ to VDCX-	5.6	mm
		From U,V,W to Baseplate	12	mm
		From VDCX+,VDCX- to Baseplate	12.5	mm
		From Gate driver HS,LS to Primary	4.5	mm
		From Gate driver Primary to U,V,W	>15	mm
		From Gate driver HS,LS to VDCX+,VDCX-	>15	mm
CTI-Comparative Tracking Index		Power module	min 175	
Mounting Torque	M_P	Terminals VDCX+, VDCX-, U,V,W	4	N-m
	M_{BP}	Baseplate	2	N-m

[4] Package resistance temperature coefficient: 0.39%/°C

Max Absolute Ratings

"Gate Driver"

Parameter	Min.	Max.	Units
VCC-GND	-0.5	18	V
PWM-XT/PWM-XB/RSTN wrt GND	-0.5V	5.5	V
FLT-B-U/ FLT-T-V/FLT-W wrt GND	-0.5V	18	V
CTI-Comparative Tracking Index	175		
Junction Temperature		175	°C
Storage and Operating Temperature	-40	125	°C
ESD Rating (Human Body Model) between VCC/GND/PWM-XT/PWM-XB/RSTN/FLT-X pins[5]	1.5		kV

Isolation

Parameter	Condition	Min.	Typ.	Max.	Units
Any of "VDCX+/VDCX-/U/V/W/VCC/GND/PWM-XT/PWM-XB/FLT-X wrt to baseplate	DC (for 1mn)		5000		V
	@ 1000VDC		>1		GΩ
VDCX+/VDCX-/U/V/W wrt to VCC/GND/PWM-XT/PWM-XB/FLT-X	DC (for 1mn)		3000		V
	@ 1000VDC		>20		MΩ
Parasitic capacitance	Between high-side and primary (per phase)		11		pF

DC Bus Voltage Monitoring[6]

Parameter	Symbol	Condition	Typ	Unit
DC BUS voltage monitoring output	VDCM		0.0033*Diff(VDCV+,VDCU-)	V
Isolation Resistance between VDCM and VDCV+/VDCU-		1200VDC; 175°C	>20	MΩ

Temperature Monitoring

Parameter	Symbol	Condition	Typ	Unit
Temperature monitoring output	TEMP-U TEMP-V TEMP-W		$NTC_{R\,(Ohm)}$*5/($NTC_{R\,(Ohm)}$+1500)	V
NTC resistance	NTC_R	T_{NTC}=25°C	5000	Ω
NTC isolation wrt power device terminals[7]		1200VDC; 175°C	>10	GΩ

Steinhart-Hart Coefficients for NTC_R versus Temperature computation:

$$1/(T_{NTC}-273.15) = A+B*\ln(R)+C*\ln^3(R)$$

	A	B	C
T_{NTC}< (273.15+25)K	$9.931*10^{-4}$	$2.658*10^{-4}$	$1.563*10^{-7}$
T_{NTC}> (273.15+25)K	$9.923*10^{-4}$	$2.664*10^{-4}$	$1.496*10^{-7}$

[5] Because of functional isolation requirement between «VDCX+/VDCX-/U/V/W» and « VCC/GND/PWM-XT/PWM-XB/FLT-X » pins, no ESD performance can be guaranteed between those 2 pin groups.
[6] There is no galvanic isolation on this measurement but monitored voltage goes through four 5 MOhms resistors (respecting 4.5 mm creepage over the resistor chain); at 1200V, there is a max current of 60µA
[7] Isolation is provided by the gel inside the power module

Electrical Characteristics "Power module"

Unless otherwise stated: (VCC-GND)=15V, T_C=25°C. **Bold underlined** values indicate values over the whole temperature range (-40°C < T_J < +175°C).

"SiC Power MOSFET's"

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Threshold voltage	V_{TH}	T_j=25°C ; I_{DS} = 0.02A; V_{DS} = V_{GS}	1.8	2.15	3.5	V
		T_j=175°C ; I_{DS} = 0.02A; V_{DS} = V_{GS}		1.7		V
Drain cut-off current	I_{DSS}	V_{GS} =-3V, V_{DS}=1200V, T_j=25°C		1		µA
		V_{GS} =-3V, V_{DS} =1200V, T_j=175°C		50		µA
Static drain-to-source resistance[8]	R_{DSon}	V_{GS} =15V, ID=300A, T_j=25°C		3.25	4	mΩ
		V_{GS} =15V, ID=300A, T_j=175°C		5.15		mΩ
Breakdown drain-to-source voltage (DC characterization)	V_{BRDS}	V_{GS} =-3V; I_{DS} = 500 µA	**1200**			V
Input capacitance	C_{ISS}	V_{GS} =0V_{DC}, V_{DS} =600V_{DC} f = 100 kHz V_{AC} = 25mV		30		nF
Output capacitance	C_{OSS}			1.3		nF
Feedback capacitance	C_{RSS}			76		pF
Turn-on delay time	$T_{d(ON)}$	V_{DS}=600V; V_{GS}= -3/15V; I_{DS} = 300A; L = 50µH		74		ns
Rise time	T_r			104		ns
Turn-off delay time	$T_{d(OFF)}$			213		ns
Fall time	T_f			40		ns
Turn-On Switching Energy	E_{on}			8.42		mJ
Turn-Off Switching Energy	E_{off}			7.05		mJ
Gate to Source Charge	Q_{GS}	Tj=25°C ;V_{DS}= 600V; I_{DS} = 300A; V_{GS} = -3/15V		292		nC
Gate to Drain Charge	Q_{GD}			285		nC
Total Gate Charge	Q_G			910		nC
Short-circuit protection threshold	I_{SCth}	$T_{J=}$25°C		1145		A
		$T_{J=}$175°C		750		A
Maximum short-circuit duration	t_{SC}			2		µs

"SiC Reverse Diode"

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Diode Forward Voltage	V_F	T_j=25°C ; I_{SD} = 300A; V_{GS} =-3V		5.18		V
		T_j=175°C ; I_{SD} = 300A; V_{GS} =-3V		4.5		V
Continuous Diode Forward Current	$I_{SD,DC}$	V_{GS} =-3V, T_c=25°C, Tj<175°C		280		A
Diode Pulse Current	$I_{SD, Pulse}$	V_{GS} =-3V, pulse width t_p limited by T_{jmax}		720		A
Reverse Recovery Time	t_{RR}	V_{DS}=600V; V_{GS}= -3V; I_{SD} = 300A Tj=25°C;L = 50µH; dI/dt= 8.9A		28		ns
Reverse Recovery Charge	Q_{RR}			1.58		µC
Peak Reverse Recovery Current	I_{RR}			88		A
Reverse Recovery Energy	E_{RR}			0.26		mJ

Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Junction-to-Fluid Thermal resistance[9]	Θ_{JF}	Each switch position		0.165		°C/W
Junction-to-Case Thermal resistance	Θ_{JC}	Each switch position		0.13		°C/W
Operating Junction Temperature					**<u>175</u>**	°C

[8] R_{DSon} does not include package resistance; see section Max Absolute Ratings for information about package resistance

[9] Measurement conditions: Flow rate: 10l/min; 50% ethylene glycol, 50% water, 75°C inflow temperature. Reference cooler design available upon request.

Electrical Characteristics "Gate Driver"

Unless otherwise stated: (VCC-GND)=15V, T_C=25°C. **Bold underlined** values indicate values over the whole temperature range (-40°C < T_J < +175°C).

Parameter	Condition	Min	Typ	Max	Units
Gate driver power supply					
VCC		**12**	**15**	**18**	V
I_{VCC}	0 kHz PWM; VCC=15V		170		mA
	25 kHz PWM; VCC=15V; VDCX+ = 0V		380		mA
	25 kHz PWM; VCC=15V; VDCX+ = 600V;		490		mA
PWM-XL/PWM-XH/RSTN inputs					
V_{IH}	Applies to PWM-XB/PWM-XT/RSTN		3.5		V
V_{IL}			1.6		V
Hysteresis			1.9		V
Pull-down impedance (PWM-XB/PWM-XT)/ pull-up impedance (RSTN)			2		kΩ
FLT-X open drain outputs					
On resistance				**25**	Ω
Voltage on FLT-X				**18**	V
Internal pull-up resistance	Connected between FLT-X and VCC		10		kΩ
Minimum external pull-up resistance			300		Ω
Output Fall Time (90% to 10%)	On 50 pF external capacitance External pull-up: 300 Ohm to VCC		36		ns
Non-overlap delay (NOV_D)					
Non Overlap delay HIGH => LOW	In Local Mode (JP1="ON") Measured at power switch gate		400		ns
Non Overlap delay LOW => HIGH			350		ns
PWM data path					
PWM frequency[10]				**50**	kHz
Duty cycle		**0**		**100**	%
Anti-glitch filter window			500		ns
Propagation delay (PWM-XB/PWM-XT →U/V/W) (50% to 10%)	Direct Mode; excluding anti-glitch filter delay		180		ns
Propagation delay (PWM-XB/PWM-XT → U/V/W) (50% to 10%)	Local Mode; excluding anti-glitch filter delay		600		ns
Fault latching time					
Timer value (Primary or Secondary faults)			14		ms
Timer variation		-30		+25	%
Under-voltage Lockout on VCC (UVLO_P)					
UVLO_P High Threshold			9.75		V
UVLO_P Low Threshold			8.2		V
Delay from UVLO_P detection to FLT-X @ fault level			200		ns
Under-voltage Lockout on secondaries gate driver supplies(UVLO_S)					
UVLO_S High Threshold			16.8		V
UVLO_S Low Threshold			15.5		V
Delay from UVLO_S detection to FLT-X @ fault level			600		ns
Desaturation detection (DESAT_H, DESAT_L)					
Desaturation Threshold	wrt to power switch source		4.6		V
Desaturation Blanking time			1		µs
Delay from Desaturation detection to FLT-X in fault state			600		ns
Soft Shutdown gate fall time	V_{GS} from 15V to 0V		1		µs

[10] Please refer to section
Gate driver temperature derating for operation above 25kHz (page 17)

Typical performances (per switch)

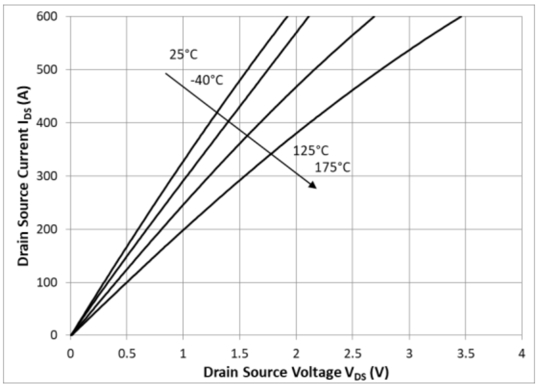


Figure 1: Drain current vs V_{DS} (V_{GS}=15V, t_p < 200µs)[11]

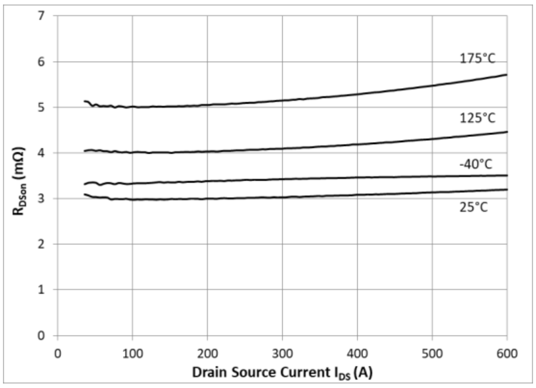


Figure 2: On-state drain source resistance vs. Drain current (V_{GS} =15V, t_p < 200µs)[11]

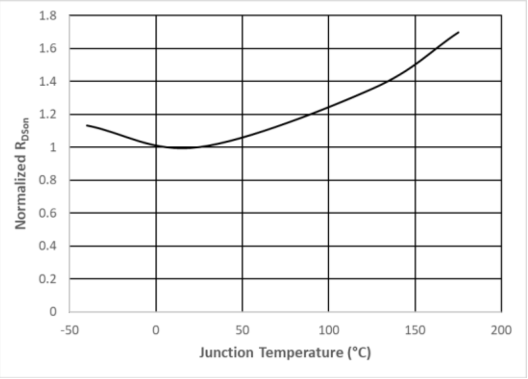


Figure 3: Normalized on-state drain source resistance (I_{DS}=300A, V_{GS} =15V, t_p < 200µs)[11]

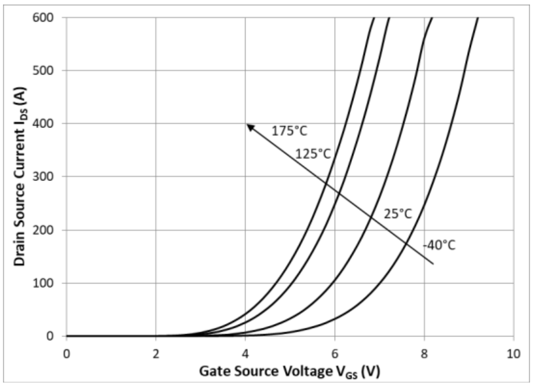


Figure 4: Drain current vs V_{GS} voltage (V_{DS}=20V, t_p < 200µs)

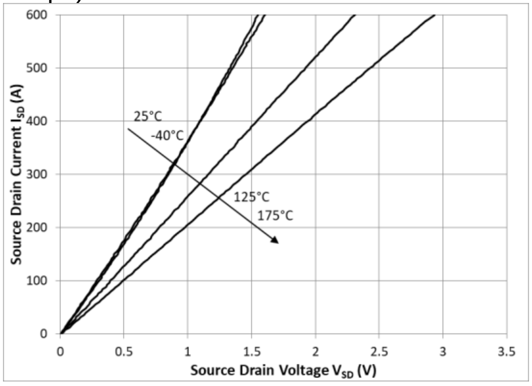


Figure 5 : 3rd quadrant characteristics (V_{GS}=15V, t_p < 200µs) [11]

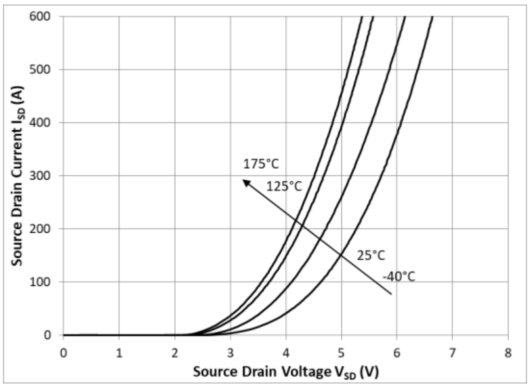


Figure 6: 3rd quadrant characteristics (V_{GS}=-3V, t_p < 200µs) [11]

[11] Package resistance excluded

Typical performances (per switch) (cnt'd)

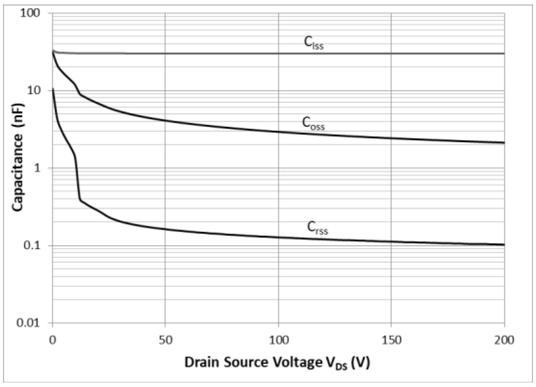


Figure 7: Typical capacitances vs V_{DS} (T_j=25°C ; f = 100 kHz, V_{AC} =25mV)

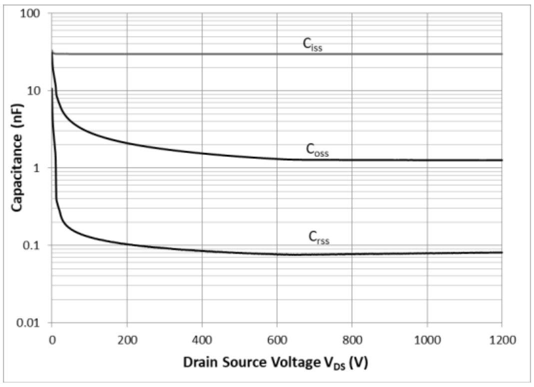


Figure 8 : Typical capacitances vs V_{DS} (T_j=25°C ; f = 100 kHz, V_{AC} =25mV)

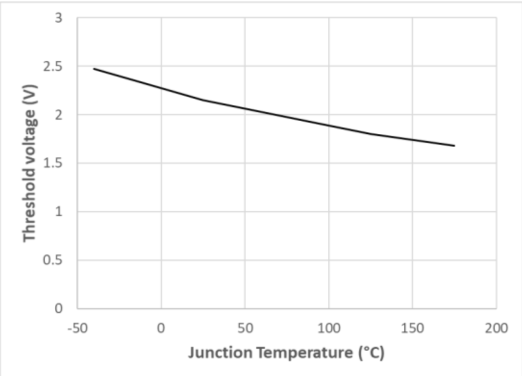


Figure 9:Threshold vs temp (I_{DS}=20mA; V_{GS}=V_{DS})

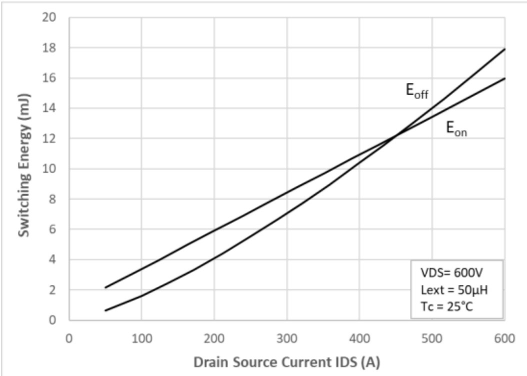


Figure 10 : Switching Energy

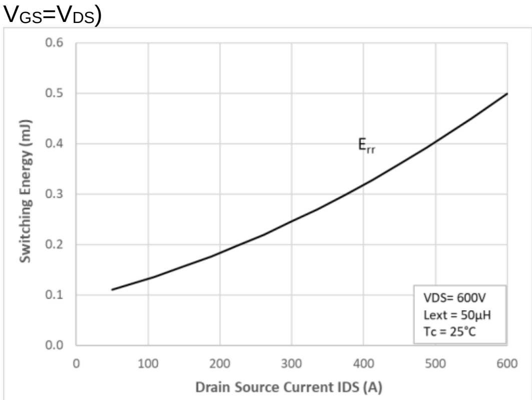


Figure 11 : Reverse Recovery Energy

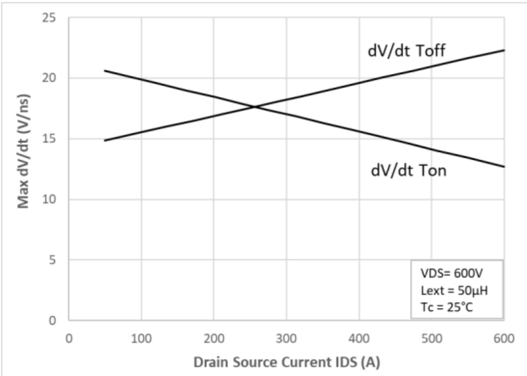


Figure 12 : Max dV/dt vs Drain current

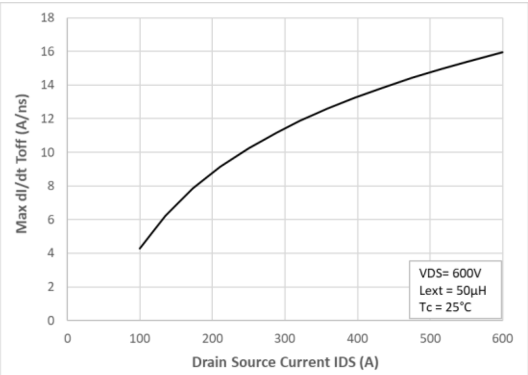


Figure 13 : Max Turn-off dI/dt vs Drain current

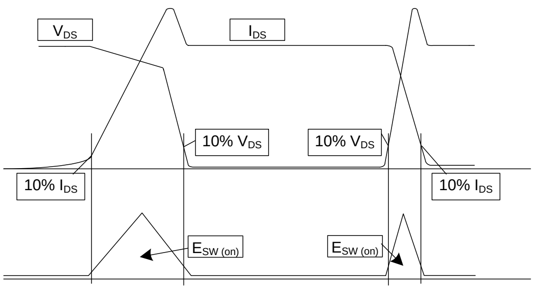


Figure 14 : Switching energy computation

Typical performances (per switch) (cnt'd)

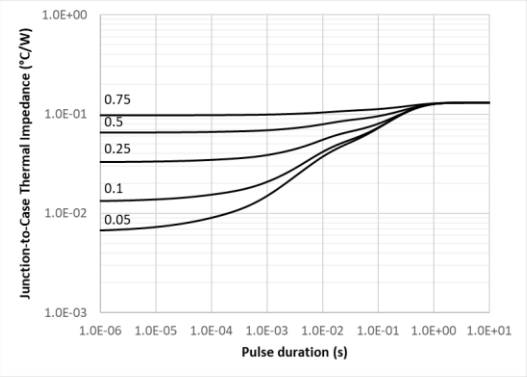


Figure 15: MOSFET Junction to Case Thermal Impedance

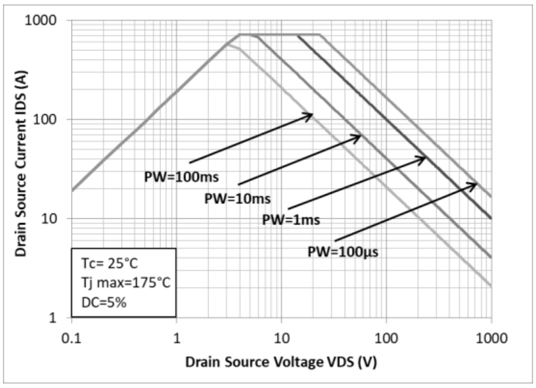


Figure 16: Forward Bias Safe Operating Area (FBSOA)

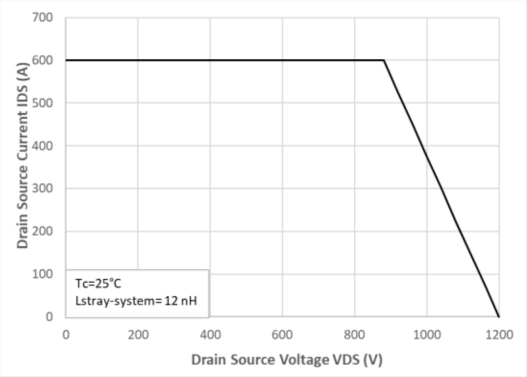


Figure 17 : Reverse Bias Safe Operating Area (RBSOA)

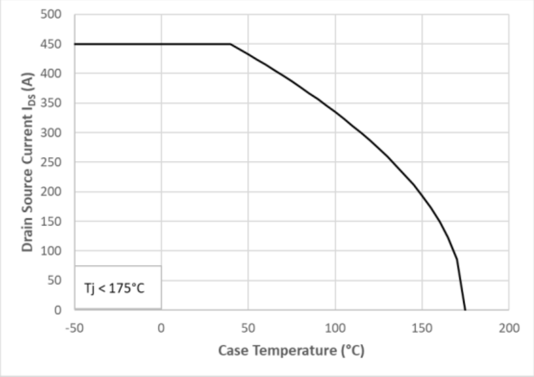


Figure 18: Continuous Drain Current Derating vs Case temperature

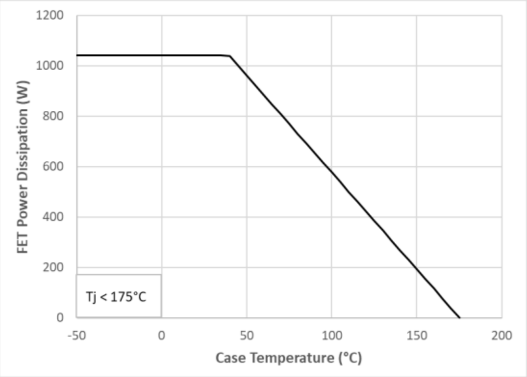


Figure 19 : Maximum Power Dissipation Derating vs Case temperature

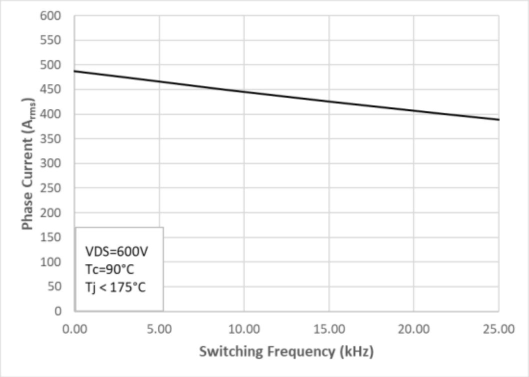


Figure 20 : Maximum Phase Current Capability vs Switching Frequency (Inverter Application)

Gate Driver Circuit Functionality

Description

Main features of the CXT-PLA3SA12450A gate driver are:

- Isolated data transmission (robust to high dV/dt) (data and fault) on both high and low side channels
- Adjustable fault timer with automatic restart
- Safe start-up sequence through monitoring of the main supply (UVLO) and of the voltage regulators output (through Power-Good function)
- Permanent and programmable Under-Voltage Lockout (UVLO) monitoring on external and internally generated power switch supplies
- Desaturation detection function with programmable blanking time and threshold protecting power switches in case of abnormal current levels
- Soft-Shutdown transistor and control performing power device graceful shutdown in case of fault and so preventing too high dI/dt in the power stage
- Flyback DC-DC converter (one per phase) with cycle-by-cycle current limit for short circuit protection
- High-precision (typ 3%) high-level gate voltage generation
- Single-ended Schmitt-trigger PWM inputs
- Open-drain low-ohmic (typ. 25Ω) fault output
- Support of 2 separate incoming PWM channels and of locally generated non-overlapped PWM signals (per phase) (configuration via jumper)
- Configurable 500ns (typ) spike filter on incoming PWM signal for enhanced noise robustness
- Anti-overlap protection on incoming PWM signals
- Gate-2-Source short-circuit protection
- Support of 100% duty-cycle PWM
- Very low parasitic capacitance between secondaries and primary

Under-Voltage Lockout (UVLO)

CXT-PLA3SA12450A gate driver board monitors constantly:

- VCC power supply
- High-side secondary supplies (typ +15V/-3V)
- Low-side secondary supplies (typ +15V/-3V)

At primary side, the monitored power supply is “VCC-GND”; to avoid oscillation when (VCC-GND) is close to the UVLO threshold, a hysteresis is implemented.

At each secondary side, the monitored power supply is “VDD_L-VSS_L”/ “VDD_H-VSS_H”; to avoid oscillation when (VDD_x-VSS_x) is close to the UVLO threshold, a hysteresis is implemented.

Refer to the chapter Fault Management for details about fault behavior and management.

On-board power supplies

The on-board isolated power supply (per phase) is a regulated flyback DC-DC converter providing both high-side and low-side channels with the positive and negative supply voltages required to drive the power FETs. It offers high voltage isolation between the channels, high dV/dt sustainability and very low parasitic capacitance. Cycle-by-cycle current monitoring at primary side is implemented to protect the board against short-circuit.

High accuracy (typ 3%) is achieved on all secondary positive supplies.

Interface towards controller

PWM inputs

PWM-XB and PWM-XT input interface is based on 5V Schmitt-Trigger input receivers and is Active High. Active Low is available as an option.

CXT-PLA3SA12450A gate driver board implements 2 protection functions on the PWM data paths:

- Anti-glitch: any negative or positive glitch on PWM-XB/PMW-XT signals smaller than a programmed value is ignored by the board; this is increasing immunity of incoming signals against external noise; the PWM signals are delayed by the corresponding anti-glitch time

  t_{MINPW} (ns)= 1* [C_{GLIx} (pF)]

- Anti-overlap: this circuit prevents PWM-XB and PMWH from being active at the same time.

FAULT outputs

The output buffers operate as an open-drain driver with a very low Ron resistance (typ. 25Ω), enabling the use of low value pull-up resistance for increased noise immunity.
An on-board 10k pull-up resistance (connected to internal 5V supply) is present on each fault output to ease initial testing.
By default, there is one fault output per side [top/bottom] (one fault per phase is available as an option[12]).

Isolated data transmission

CXT-PLA3SA12450A gate driver board uses integrated digital isolators. Those devices provide isolation, immunity against high dV/dt and low parasitic capacitance.
In case no power supply is present at the secondary side, a fault is generated at the primary side.

Desaturation detection

The purpose of the desaturation function is to detect that the voltage at the drain of the power switch, in "ON" state, is higher than a given threshold. This informs the logic part of the system about possible damage of the power arm (e.g. a short circuit at the arm level leading to an overcurrent in the power switch).

The sensing of the power device drain voltage is performed through a high voltage sensing diode whom cathode is connected to the power switch drain and whom anode is connected to a current source (typ 2mA) and a sensing circuit.

When DC power terminals are neither connected nor powered externally, per phase circuit, the gate driver DESAT function will biais the power terminals "VDCx+" – "VDCx-" to 19V through a 15 kOhm impedance.

The desaturation threshold (voltage on transistor VDS) is configured by on-board resistors and can be tuned according to the table below.

Rdesat value	Desat threshold (V)	
	25°C	125°C
0KΩ	1.18	1.47
5KΩ	2.6	2.87
10KΩ	4.01	4.27
12KΩ (default)	4.6	4.83
15KΩ	5.42	5.66
20KΩ	6.84	7.06

At system level, the de-saturation detection should only be taken into account after a defined time following the low-to-high transition on the power device gate. This "blanking" time t_{DESAT_D} is implemented and adjusted by an on-board capacitor C_{DESATD} (68pF installed) and can be calculated as follows:

t_{DESATD} (ns)= 14* [C_{DESATD} (pF) + 7]

If after t_{DESAT_D} time, the DESAT comparator output indicates that the transistor VDS level is higher than the programmed threshold value, an internal DESAT fault is generated. Refer to the chapter Fault

[12] Contact CISSOID if you require this option

Management for details about fault behavior and management.
When the desaturation fault is detected, the power module gate is gracefully discharged thanks to the Soft-Shutdown circuit to avoid high dI/dt at power module turn-off

Active Miller Clamping

In case of high positive dV/dt and despite the negative drive of the power module gate, a parasitic turn-on of the gate could take place, inducing shoot-through current on the power arm.
To prevent this, CXT-PLA3SA12450A gate driver board implements an Active Miller Clamping function by bypassing the gate resistance with a low ohmic path (implemented with a transistor) when the gate is driven negative.
This transistor also helps to limit the amplitude of negative kick on the power module gate in case of negative dV/dt.

Fault Management

Fault management is taking place on each phase independently.
At **primary side**, fault is generated by any of those situations:

- Main power supply (VCC) is below the UVLO threshold
- Primary linear voltage regulator (generating the 5V output required by the on-board logic) is below the internal Power Good level

Those faults are internally combined to generate a unique fault signal. This internal primary fault signal is latched for 14msec.

While the fault is latched:

- Both FLT-X pins are tied to "0"
- Both power switches are turned off
- On board DC-DC Converter is off

After the predefined latch time period, the phase controller will attempt to return to normal operation:
- If the fault is still present, the phase will stay in the fault state till the fault disappears
- If the fault disappeared (e.g. temporary UVLO situation), the phase will go out of FAULT state and return to normal operation (DC-DC converter turned on and data paths active); still, on the PWM path, transition to normal operation will happen on the next positive edge of the incoming PWM signal.

The primary fault state is combined with the faults returned by the secondary devices according to Table 1.

At **each of the secondary side**, fault is generated by any of those situations:

- Power supply is below the UVLO threshold
- Secondary voltage regulator (5V) output voltage is below the Power-Good threshold
- Desaturation situation is detected by the DESAT comparator

Those faults are internally combined to generate a unique fault signal. This internal fault signal is latched for 14msec.
While the fault is latched, the gate driver is turned off. At the transition between "no fault" and "fault" situation, the gate driver circuit is gracefully shut down.

After the predefined latch time period, the gate driver circuit returns to normal operation:

- If the fault is still present, the gate driver is kept turned off till the fault disappears
- If the fault disappeared (e.g. temporary UVLO situation), normal operation will resume on the next positive edge of incoming PWM signal

Prim fault	Low-side fault	High-side fault	FLT-B-U (Bottom)	FLT-T-V (Top)
No	No	No	High-Z (pulled up)	High-Z (pulled up)
No	Yes	No	Pulled down	High-Z (pulled up)
No	No	Yes	High-Z (pulled up)	Pulled down
No	Yes	Yes	Pulled down	Pulled down
Yes	Yes or No	Yes or No	Pulled down	Pulled down

Table 1: FAULT aggregation table (Default option:reporting per side)

-

Prim fault	Low-side fault	High-side fault	FLT-X
No	No	No	High-Z (pulled up)
No	Yes	No	Pulled down
No	No	Yes	Pulled down
No	Yes	Yes	Pulled down
Yes	Yes or No	Yes or No	Pulled down

Table 2: FAULT aggregation table (reporting per phase option)

RSTN (Reset) behaviour

While in Low-State, pin RSTN forces all PWM input signals to “0”, turning off all SiC MOSFET gates in Direct mode and turning off the High-Side SiC MOSFET and keeping Low-Side SiC MOSFET on in Local Mode

Protections

CXT-PLA3SA12450A gate driver is protected on each channel against:

- Gate overvoltage
- Gate undervoltage
- Gate-source permanent short-circuit

Non-Overlap Generation

CXT-PLA3SA12450A gate driver board offers 2 modes of operation:

- Direct Mode: PWM-XB and PWM-XT are generated independently outside CXT-PLA3SA12450A gate driver board. In this case, proper non overlapping must be generated externally.
- Local Mode: PWM-XB and PWM-XT are generated from one input signal (PWM-XT) and proper non overlapping timing is managed locally on each phase of CXT-PLA3SA12450A gate driver board (cfr Figure 21)

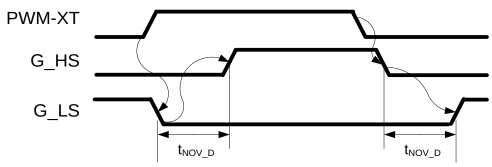


Figure 21: Local Mode operation

The choice between those 2 modes of operation is made via the 2 pin header jumper JP1 (located at primary side, one per phase):

- JP1 ON: Local mode
- JP1 OFF: Direct mode

When in Local Mode, an on-board capacitance (Cnovd) defines the non-overlap delay according to following formula:

$$t_{NOV\_D}\,(ns)=5.5 * C_{NOVD}(pF)$$

Board power dissipation

Current consumption of the CXT-PLA3SA12450A gate driver board (VCC=15V; VDCX+=0V) can be computed as follows:

$$Iin = 170mA + 8.4 * Fs$$

Where:

- Iin: Input current (in mA) (wrt to VCC = 15V)
- Fs: Switching frequency (in kHz)

The duty cycle of the PWM-XB/PWM-XT signals has almost no influence on the current consumption (assuming PWM-XB and PWM-XT duty cycles are complementary).

To stay within specifications of the internal secondary voltages, the maximum average Iin current should be 1000 mA (for VCC =15V).

Temperature measurement

Temperature of each phase is measured using an NTC resistance mounted on the power module DBC.

The NTC resistance variation with respect to temperature is reported in Figure 22: NTC resistance vs tempand obeys to the formula provided in section Max Absolute Ratings.

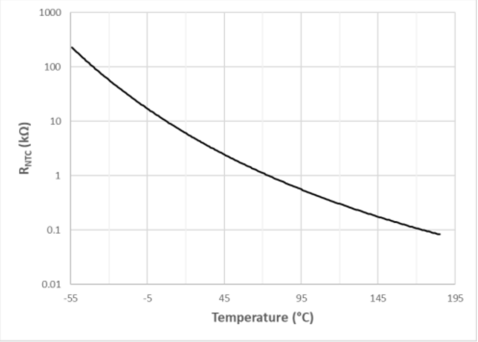


Figure 22: NTC resistance vs temp

The NTC resistance value is converted into an analog voltage fed to the connector pins TEMP-U, TEMP-V, TEMP-W. Figure 23: TEMP-X voltage vs tempshows the relationship between TEMP-X voltage and NTC temperature.

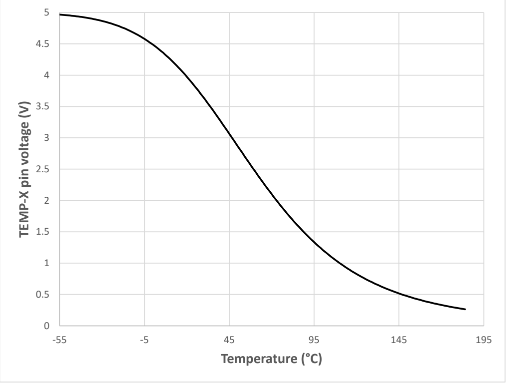


Figure 23: TEMP-X voltage vs temp

Gate driver temperature derating

The CXT-PLA3SA12450A gate driver has been designed to operate at 125°C ambient upto 25kHz switching frequency. Above 25 kHz, a derating according to the graph below needs to be applied.

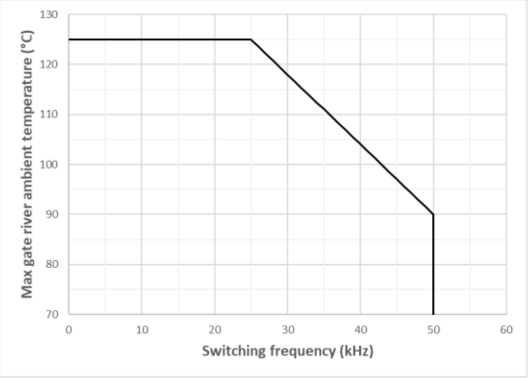


Figure 24: Gate driver temperature derating

Timing Diagrams

Figure 25 illustrates the CXT-PLA3SA12450A gate driver board low-side driver dynamic behavior in normal operation and fault conditions.

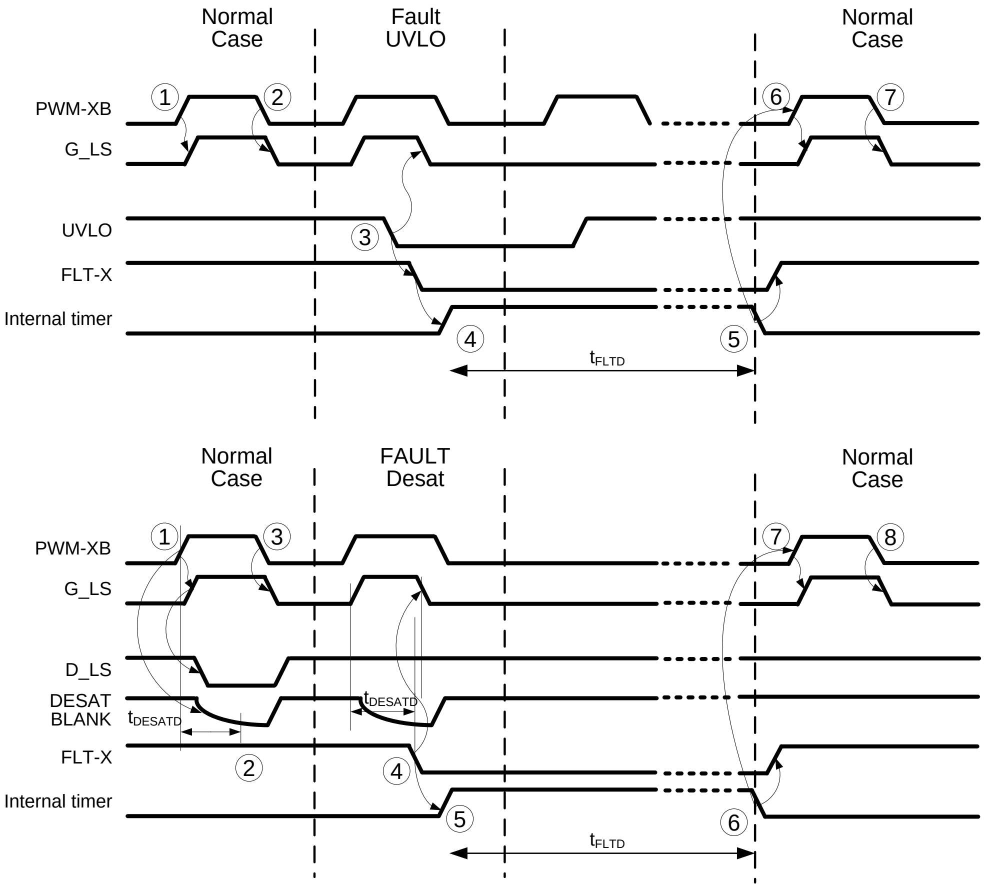


Figure 25: Timing diagram CXT-PLA3SA12450A low-side gate driver behaviour

In Normal operation

On PWM-XB rising edge (1), rising edge is generated on G_LS (after propagation delay through CXT-PLA3SA12450A gate driver board).
After rising edge on G_LS, low-side power module is turned ON and midpoint node is going to "0" state (voltage equals to Ron * current flowing through the power device).
D_LS node is also pulled down and after blanking time (t_{DESAT_D}), no desaturation fault is detected and FLT-X remains high.

On PWM-XB falling edge (2), falling edge is generated on G_LS (after propagation delay through CXT-PLA3SA12450A gate driver board)
After falling edge on G_LS, the low-side power device is turned OFF.

In DESAT fault situation

On PWM-XB rising edge (3), rising edge is generated on G_LS (after propagation delay through CXT-PLA3SA12450A gate driver board)
After rising edge on G_LS, low-side power module is turned ON; because of a desaturation fault, D_LS node does not reach its normal "0" level. Thanks to the DESAT comparator, CXT-PLA3SA12450A gate driver board detects this fault situation and turns off gracefully G_LS. Power device is turned off. FLT-X signal is pulled down. Fault is cleared after fault timer expiry.

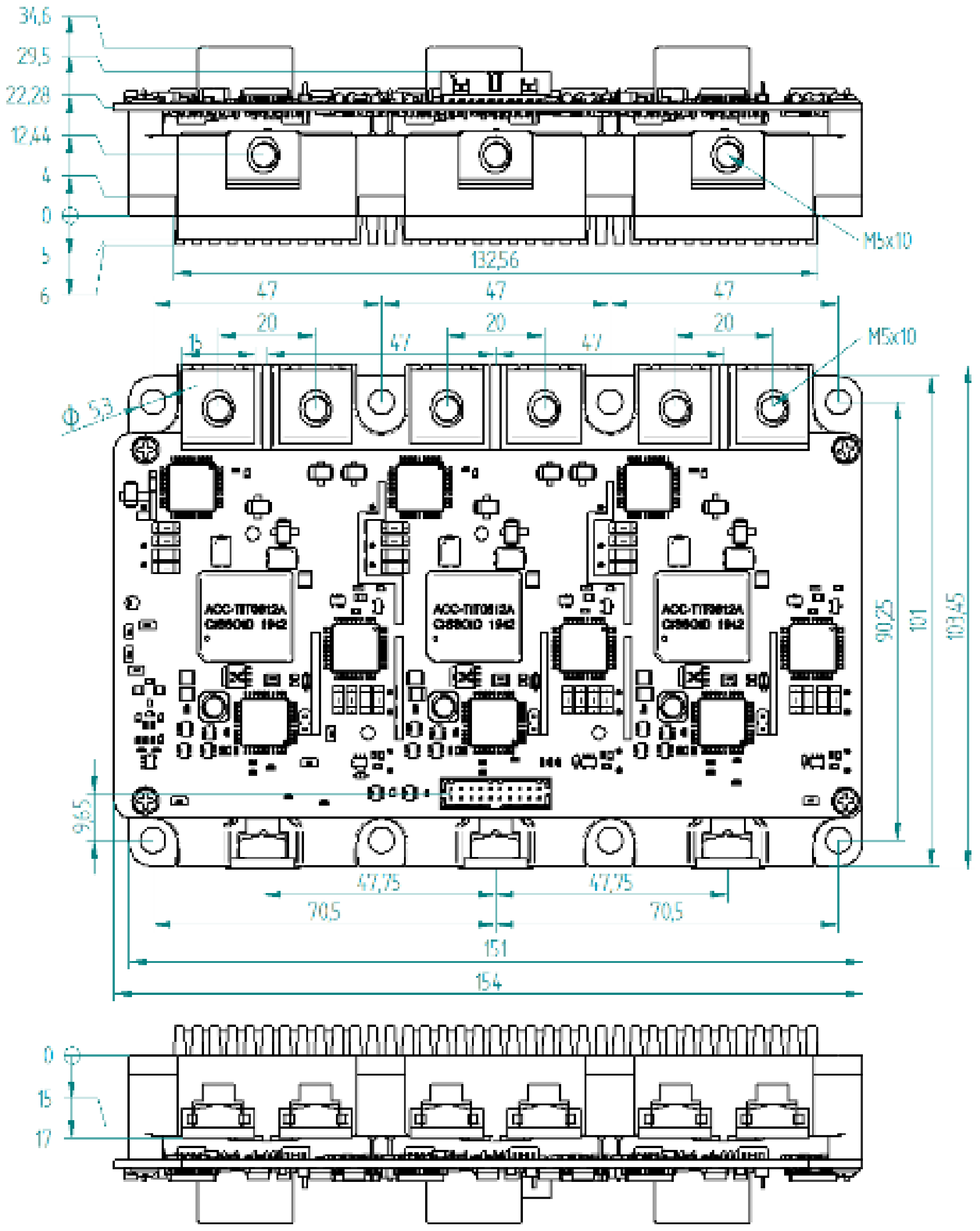
In UVLO fault situation

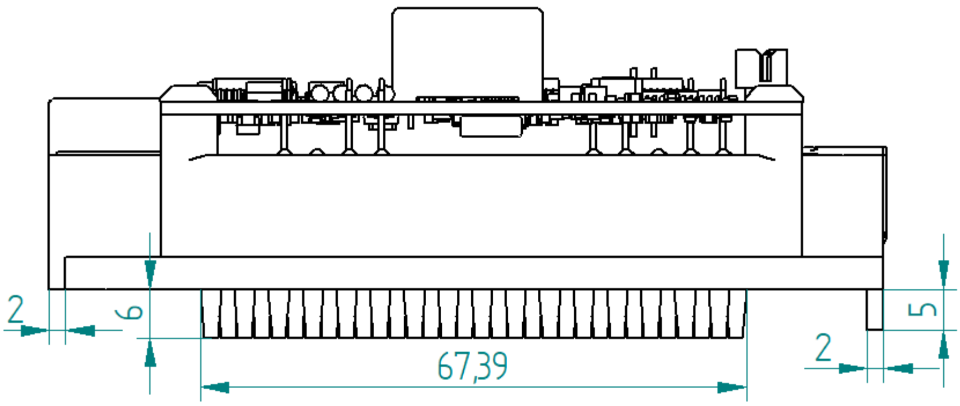
UVLO status is monitored inside the secondary devices (and inside primary device as well; for clarity, only secondary UVLO situation is described here). When UVLO comparator (5) detects an under-voltage situation, G_LS is gracefully shut down FLT-X signal is pulled down. Fault is cleared after fault timer expiry.

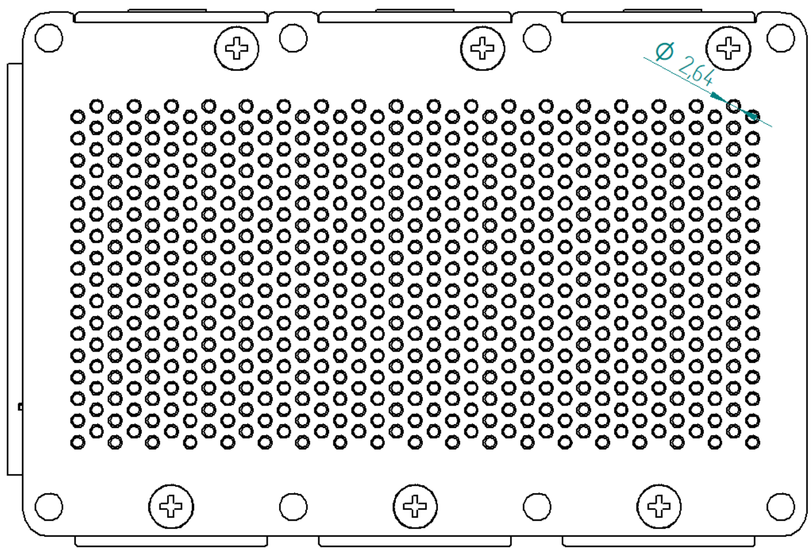
Glossary

Name	Description
D_HS	Drain of any high-side switch
S_HS	Source of any high-side switch
G_HS	Gate of any high-side switch
D_LS	Drain of any low-side switch
S_LS	Source of any low -side switch
G_LS	Gate of any low -side switch

Mechanical drawing





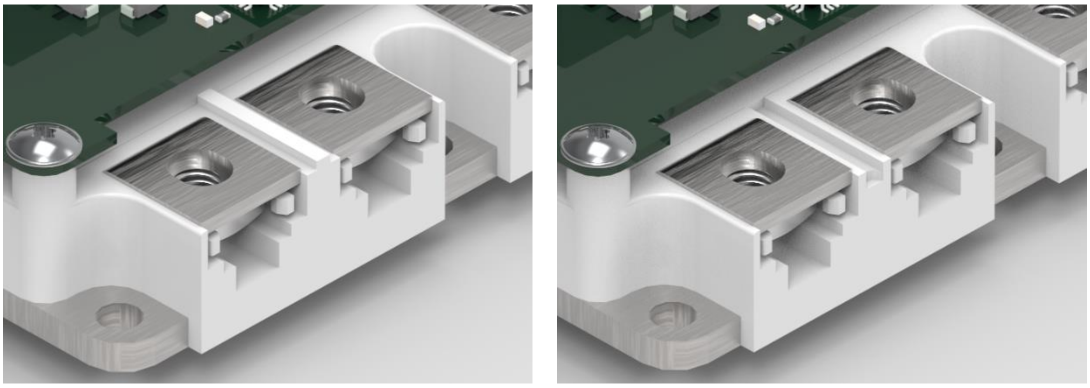


Physical dimensions (mm)
Base plate material: AlSiC
Power pins finish: Ni
Gate driver control pins finish: Au
Gate driver control connector: Molex 87831-2020

Item	Recommended reference	Comments
Baseplate fixing screws	M4x10 ISO 7380-2 A2 TX	
DC Bus Power connector bolts	M6x12 ISO 7380-2-A2-TX	Assumes min 0.7 mm DC power connector thickness
Phase power connector bolts	M6x12 ISO 7380-2-A2-TX	Assumes min 1.6 mm phase connector thickness
Gate driver female counter connector board-2-cable	Molex 51110 SERIES	
Gate driver female counter connector board-2-board	Molex 78787-2054(Tin) or 79107-7009(Gold).	

Note:

Regarding the separation between DC power terminals (VDCx+, VDCx-), 2 types of implementation may be shipped to the customer: 1 mm flanges solution or groove solution (see Figure 26 below). Both implementations meet the clearance/creepage requirements specified on page 6



Flange Groove

Figure 26: DC power terminals separation solutions

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 11 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 – F : +32 10 88 98 75 Email : sales@cissoid.com
Sales Representatives:	**Visit our website: http://www.cissoid.com**

Disclaimer

Neither CISSOID, nor any of its directors, employees or affiliates make any representations or extend any warranties of any kind, either express or implied, including but not limited to warranties of merchantability, fitness for a particular purpose, and the absence of latent or other defects, whether or not discoverable. In no event shall CISSOID, its directors, employees and affiliates be liable for direct, indirect, special, incidental or consequential damages of any kind arising out of the use of its circuits and their documentation, even if they have been advised of the possibility of such a damage. The circuits are provided "as is". CISSOID has no obligation to provide maintenance, support, updates, or modifications.

Document history

Revision	Modification	Author	Date
1.0	First version	EVZ	28-Nov-2019
1.1	Made corrections of initial version	EVZ	2-Dec-2019
1.0	First official version	EVZ	28-Feb-2020
1.1	Replace “switching loss” by “switching energy” + review switching energy numbers	EVZ	6-Apr-2020
1.2	Adapt the stray inductance value to 11.5nH after remeas-urements	EVZ	15-May-2020
1.3	Correct pinout description (pin 10: GND)	EVZ	20-May-2020
1.4	Modifications suggested by Abel: - NTC definition - RSTN pin function - Typos - Add 2 us short-circuit duration - Jumper definition	EVZ	29-Jun-2020
1.5	Modifications suggested by Sheffield University: - Mistakes in functional diagram and timing diagrams	EVZ	25-Aug-2020
1.6	Changed ref for power connection bolts (from M5 to M6) Changed figure 17	EVZ/RBE	08-Oct-2020
1.7	Correct small mistake in functional diagram	EVZ	09-Dec-2020
1.8	Add mention of “pinfin” + small changes - package resistance - module weight (gel+DBC weight is not negligible)	EVZ	30-Mar-2021
1.9	Add pressure drop graph for cooler + small bug corrections	PDE	9-Dec-2021
1.10	Update isolation definition for temp and voltage measure-ment, add mech view from power bar, change graph of max DC current and power	EVZ	29-Jan-2022
1.11	Move from fault reporting by phase to fault reporting by side Explain the use of the M5 nuts bag (compatibility with initial version of Adv Conv caps)	EVZ	13-Jun-2022
1.12	New logo	EVZ	5-sept-2023
1.13	Update for ICM REV1A DR4	EVZ	28-Feb-2024

Approvals

Recoverable Signature

X Mike Sandyck

Marketing

Signed by: 665036c6-edaa-4ea1-b7b4-b038b40726cd

Recoverable Signature

X Etienne Vanzieleghem

Engineering

Signed by: 94cd7965-ce85-4c65-840b-f2a6e514fdcf

File Name: CXT-PLA3SA12450AA-Preliminary datasheet-PDS-192038-V1.13_DRAFT