High Temperature Automotive Configurable Logic Gates Datasheet

Version: 1.3
20-Dec-23
(Last Modification Date)
(see note 1)

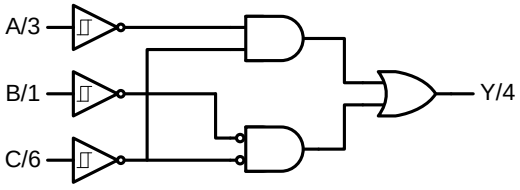
General description

The CXT-741Gxx are 4 high temperature configurable devices enabling 13 different logic functions: INV, BUFFER, AND, AND w/ inverted input, NAND, NAND w/ inverted input, OR, NOR, NOR w/ inverted input, XOR, NXOR, MUX and D Flip-Flop.

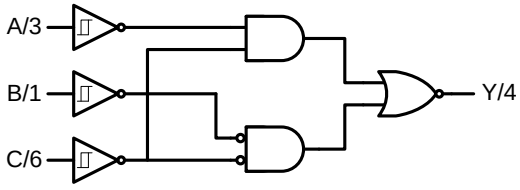
These devices are optimized for automotive applications and specified for operating junction temperature from -40°C up to +175°C (Tj), in excess of AEC-Q100 (Grade 0) qualification standard.

Features

- Operating junction temperature: from -40°C to +175°C (Tj)
- Supply voltage: 1.65V to 5.5V
- Inputs can be driven by 3.3V or 5V signals, even for lower supply voltage
- Schmitt trigger inputs for high immunity to slow changing signals
- ± 16 mA output drive current
- CMOS low power consumption
- ESD: 2000V HBM or 200V MM
- Lead Free Finish & RoHS compliant
- Tiny package: SOT-23 6 leads
- AEC-Q100 Grade 0 & PPAP capable[2]



CXT-741G57



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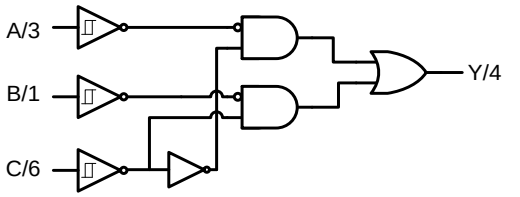

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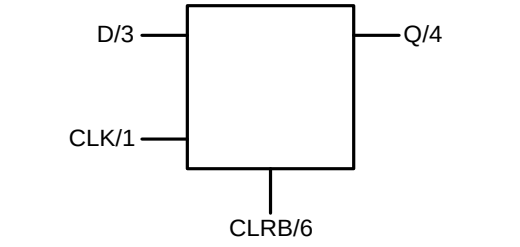

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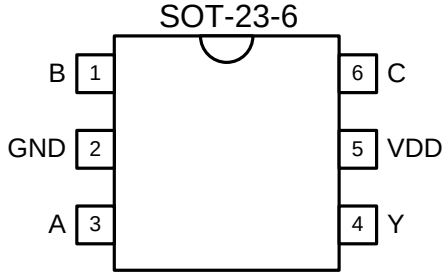
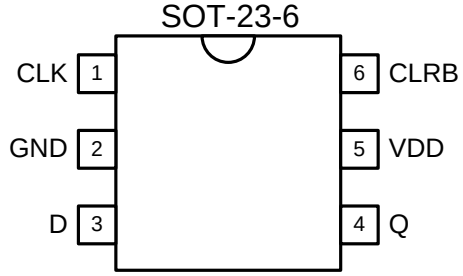


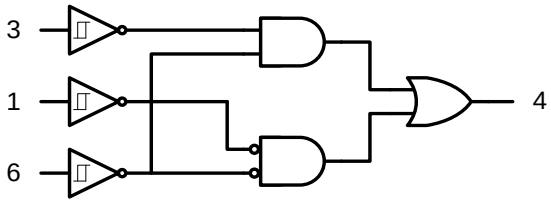


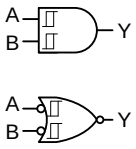
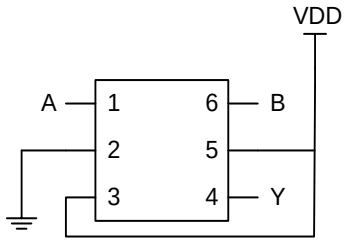
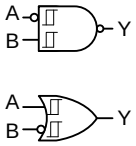
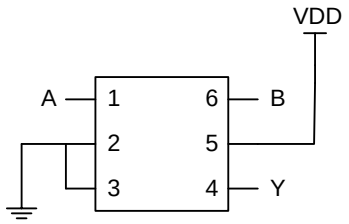
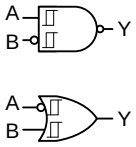
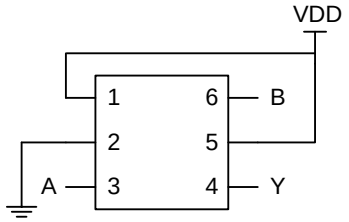
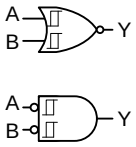
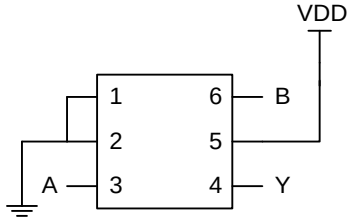
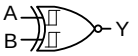
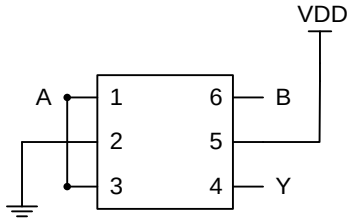
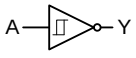
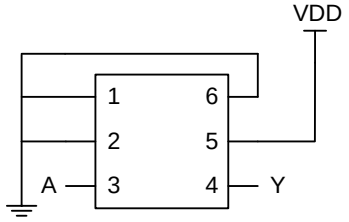
Note 1 Please always refer to the latest datasheet version available at
http://www.cissoid.com/files/files/products/galaxy/CXT-741GXX.pdf

[2] Contact CISSOID about qualification status

Logic configurations

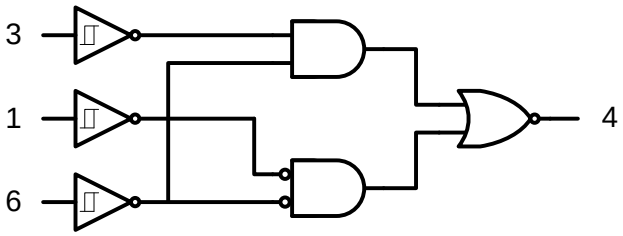
CXT-741G57

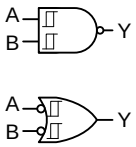
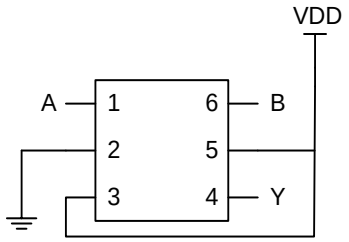
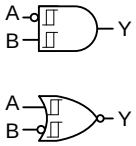
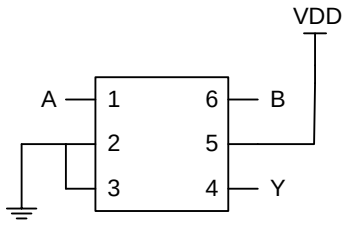
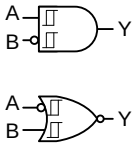
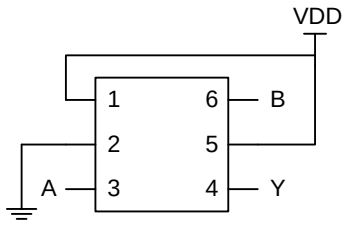
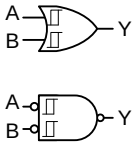
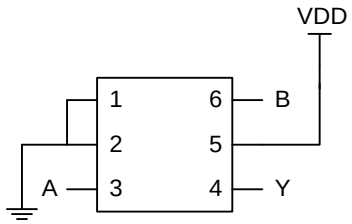
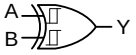
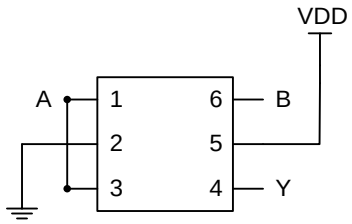
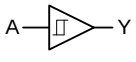
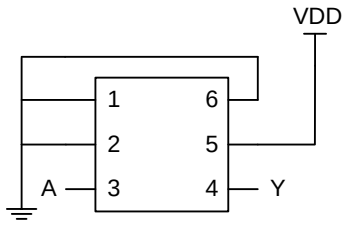


Configuration 1 2-Input AND Gate 2-Input NOR Gate with Both Inputs Inverted		
Configuration 2 2-Input NAND Gate with A Input Inverted 2-Input OR Gate with B Input Inverted		
Configuration 3 2-Input NAND Gate with B Input Inverted 2-Input OR Gate with A Input Inverted		
Configuration 4 2-Input NOR Gate 2-Input AND Gate with Both Inputs Inverted		
Configuration 5 2-Input XNOR Gate		
Configuration 6 Inverter		

Logic configurations

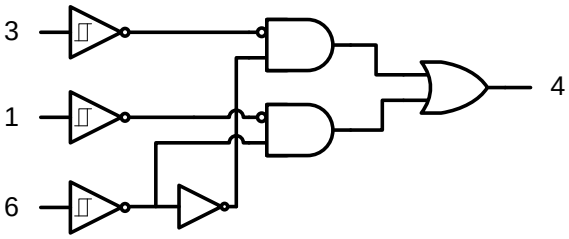
CXT-741G58

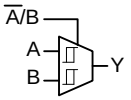
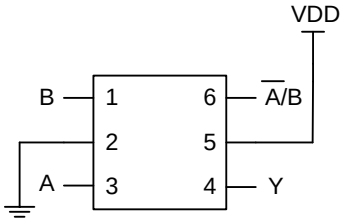
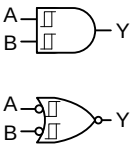
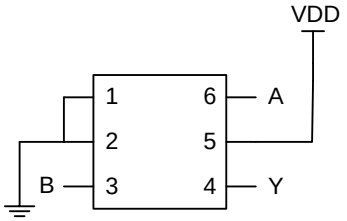
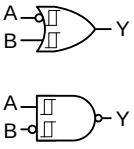
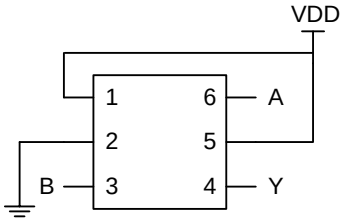
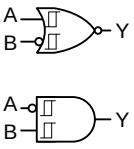
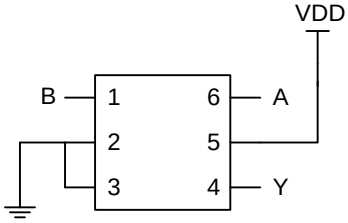
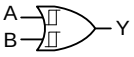
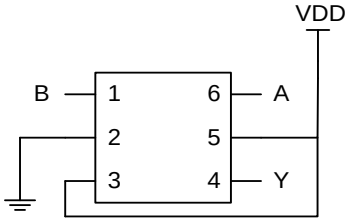
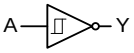
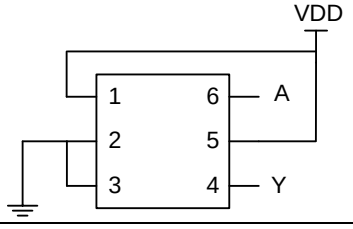


Configuration 1 2-Input NAND Gate 2-Input OR Gate with Both Inputs Inverted		
Configuration 2 2-Input AND Gate with A Input Inverted 2-Input NOR Gate with B Input Inverted		
Configuration 3 2-Input AND Gate with B Input Inverted 2-Input NOR Gate with A Input Inverted		
Configuration 4 2-Input OR Gate 2-Input NAND Gate with Both Inputs Inverted		
Configuration 5 2-Input XOR Gate		
Configuration 6 Buffer		

Logic configurations

CXT-741G97



Configuration 1 2 to 1 Multiplexer		
Configuration 2 2-Input AND Gate 2-Input NOR Gate with Both Inputs Inverted		
Configuration 3 2-Input OR Gate with A Input Inverted 2-Input NAND Gate with B Input Inverted		
Configuration 4 2-Input NOR Gate with B Input Inverted 2-Input AND Gate with A Input Inverted		
Configuration 5 2-Input OR Gate		
Configuration 6 Inverter		

CXT-741G57/CXT-741G58/CXT-741G97/CXT-741G175

Absolute Maximum Ratings(see note 3)

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage Range	-0.5	6.5	V
V_I	Input Voltage Range	-0.5	6.5	V
V_O	Voltage applied to output in high or low state	-0.3	Min(V_{DD}+0.5, 6.5V)	V
I_{IK}	Input Clamp Current (V_I<0)		-30	mA
I_{OK}	Output Clamp Current (V_O<0 V_O>V_{DD})		30	mA
I_O	Continuous Output Current		20	mA
T_J	Operating Junction Temperature	-40	175	°C
T_{STG}	Storage Temperature	-55	175	°C
ESD HBM	ESD Rating (Human Body Model)	2		kV
ESD MM	ESD Rating (Machine Model)	200		V

Operating conditions

Symbol	Parameter		Min.	Max.	Units
V_{DD}	Supply Voltage Range		-0.5	5.5	V
V_I	Input Voltage Range		-0.5	5.4	V
V_O	Voltage applied to output in high or low state		-0.3	Min(V_{DD}+0.5, 5.5V)	V
I_{OH}	High-Level Output Current	V_{DD}=1.65V		4	mA
		V_{DD}=2.3V		8	
		V_{DD}=3V		12	
		V_{DD}=4.5V		16	
I_{OL}	Low-Level Output Current	V_{DD}=1.65V		4	mA
		V_{DD}=2.3V		8	
		V_{DD}=3V		12	
		V_{DD}=4.5V		16	
$\Delta t/\Delta V_I$	Input transition rise or fall time	V_{DD}=1.8V±10%		20	ns/V
		V_{DD}=2.5V±10%		20	
		V_{DD}=3.3V±10%		10	
		V_{DD}=5V±10%		5	
T_J	Operating Junction Temperature		-40	175	°C
T_A	Operating Ambient Temperature		-40	175	°C

Electrical Characteristics

Symbol	Parameter	Test conditions	V_{DD}	Min.	Typ	Max.	Units
CI			3.3		2.7		pF
C_{PD}	Power dissipation capacitance	F= 10 MHz	1.8 to 5V		7.43		pF
ΘJA	Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout				204		°C/W
ΘJC					52		°C/W

Note 3 : Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

CXT-741G57/CXT-741G58/CXT-741G97/CXT-741G175
Electrical Characteristics

Bold underlined values indicate values over the whole temperature range (-40°C < T_J < +175°C); All typical values are at T_A=25°C

Symbol	Parameter	Test conditions	V_{DD}	Min.	Typ	Max.	Units
V_{T+}	Positive-going Input Threshold Voltage		1.8V	**1.06**		**1.26**	V
			2.5V	**1.47**		**1.68**	
			3.3V	**1.9**		**2.13**	
			5V	**2.78**		**3.04**	
V_{T-}	Negative-going Input Threshold Voltage		1.8V	**0.57**		**0.74**	V
			2.5V	**0.86**		**1.01**	
			3.3V	**1.13**		**1.35**	
			5V	**1.68**		**2.05**	
ΔV_T	Hysteresis (V_{T+}- V_{T-})		1.8V	**0.44**		**0.53**	V
			2.5V	**0.58**		**0.69**	
			3.3V	**0.71**		**0.84**	
			5V	**0.97**		**1.18**	
V_{OH}	High Level Output voltage	I_{OH}=4mA	1.65V	**1.26**			V
		I_{OH}=8mA	2.3V	**1.81**			
		I_{OH}=12mA	3V	**2.46**			
		I_{OH}=16mA	4.5V	**4.01**			
V_{OL}	Low Level Output voltage	I_{OH}=4mA	1.65V			**0.24**	V
		I_{OH}=8mA	2.3V			**0.31**	
		I_{OH}=12mA	3V			**0.36**	
		I_{OH}=16mA	4.5V			**0.35**	
I_{IN}	Input Current	V_I=5V or V_{SS}	1.65V to 5.5V			**6**	µA
I_{DD}	Supply Current	V_I=5V or V_{SS} I_O =0	1.65V to 5.5V			**8**	µA

CXT-741G57/CXT-741G58/CXT-741G97
Timing Characteristics

Bold underlined values indicate values over the whole temperature range (-40°C < T_J < +175°C); All typical values are at T_A=25°C

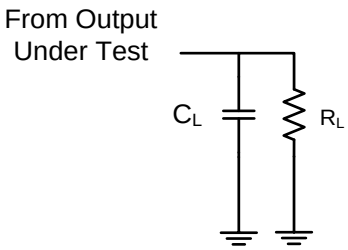
Symbol	Parameter	Test conditions	V_{DD}	Min.	Typ	Max.	Units
t_{PD}	Propagation delay from any input to output	CL=30pF RL=1KΩ	1.65V - 1.95V		12.7	**26.6**	ns
		CL=30pF RL=500Ω	2.25V - 2.75V		7.68	**15.7**	
		CL=50pF RL=500Ω	3V - 3.6V		6.38	**12.7**	
		CL=50pF RL=500Ω	4.5V - 5.5V		4.78	**8.8**	

CXT-741G175
Timing Characteristics

Bold underlined values indicate values over the whole temperature range (-40°C < T_J < +175°C); All typical values are at T_A=25°C

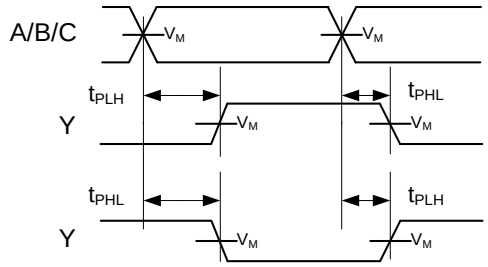
Symbol	Parameter	Test conditions	V_{DD}	Min.	Typ	Max.	Units
f_{MAX}	Maximum Frequency	CL=30pF RL=1KΩ	1.65V -1.95V	**20**			MHz
		CL=30pF RL=500Ω	2.25V - 2.75V	**35**			
		CL=50pF RL=500Ω	3V - 3.6V	**50**			
		CL=50pF RL=500Ω	4.5V - 5.5V	**70**			
t_{WCLK}	CLK Minimum Pulse Width		1.65V -1.95V	**2**			ns
			2.25V - 2.75V	**2**			
			3V - 3.6V	**2**			
			4.5V - 5.5V	**1**			
t_{WCLRB}	CLRB Minimum Pulse Width		1.65V -1.95V	**3**			ns
			2.25V - 2.75V	**2**			
			3V - 3.6V	**2**			
			4.5V - 5.5V	**2**			
t_{PD}	Propagation delay from CLK positive edge to output	CL=30pF RL=1KΩ	1.65V -1.95V			**27.43**	ns
		CL=30pF RL=500Ω	2.25V - 2.75V			**16**	
		CL=50pF RL=500Ω	3V - 3.6V			**12.98**	
		CL=50pF RL=500Ω	4.5V - 5.5V			**8.96**	
t_{PCLRB}	Propagation delay from CLRB negative edge to output	CL=30pF RL=1KΩ	1.65V -1.95V			**24.33**	ns
		CL=30pF RL=500Ω	2.25V - 2.75V			**13.65**	
		CL=50pF RL=500Ω	3V - 3.6V			**10.91**	
		CL=50pF RL=500Ω	4.5V - 5.5V			**7.8**	
t_{SU}	Setup time		1.65V -1.95V	**2**			ns
			2.25V - 2.75V	**1**			
			3V - 3.6V	**1**			
			4.5V - 5.5V	**1**			
t_h	Hold time		1.65V -1.95V	**1**			ns
			2.25V - 2.75V	**1**			
			3V - 3.6V	**1**			
			4.5V - 5.5V	**1**			

Parameter Measurement Information (notes4,5)



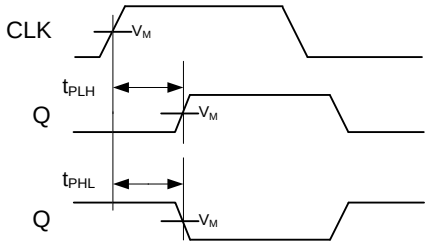
V_{DD}	Inputs		V_M	C_L	R_L
	V_I	t_r/t_f			
1.8V± 0.15V	V_{DD}	≤ 2ns	$V_{DD}/2$	30pF	1000Ω
2.5V±0.2V				30pF	500Ω
3.3V±0.3V				50pF	500Ω
5V±0.5V				50pF	500Ω

CXT-741G57/CXT-741G58/CXT-741G97

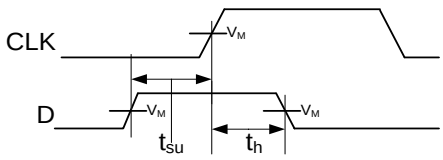


Voltage Waveform
Propagation Delay times
Inverting and Non Inverting Outputs

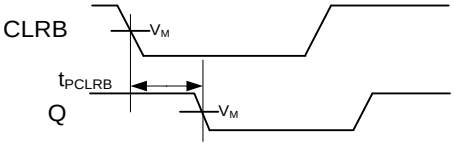
CXT-741G175



Voltage Waveform
Propagation Delay times wrt CLK



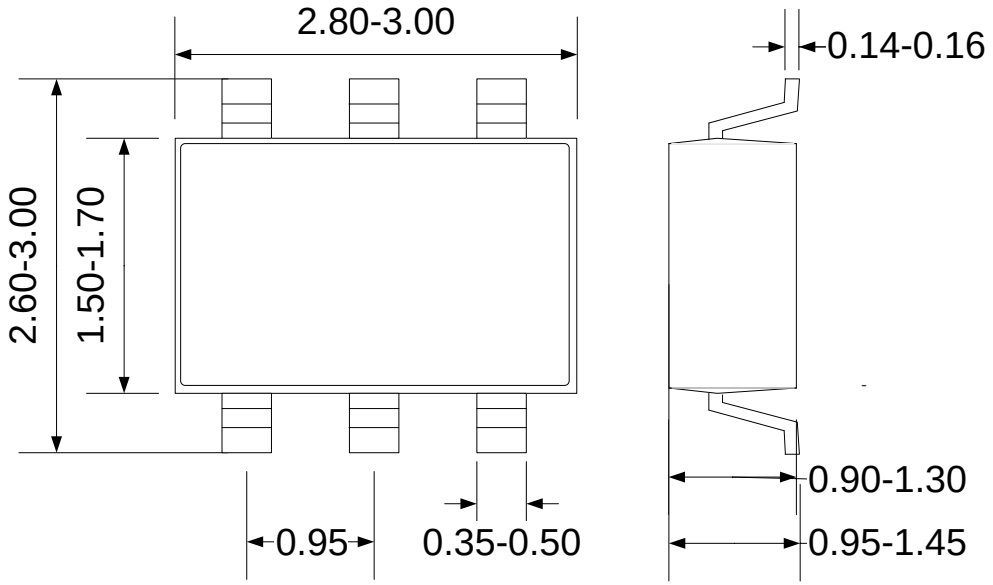
Voltage Waveform
Set-up and Hold times wrt CLK



Voltage Waveform
Propagation Delay times wrt CLRB

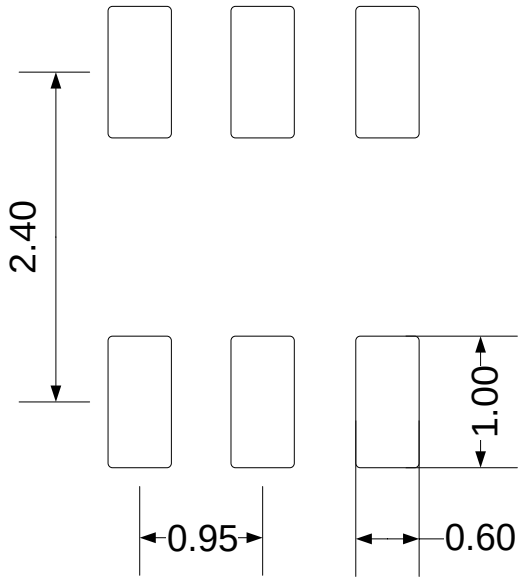
Note 4 C_L load capacitance includes PCB and probe capacitance
Note 5 : t_{PHL} and t_{PLH} are the same as t_{PD}

Package Drawing



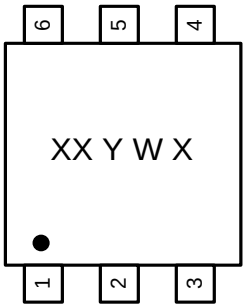
Physical dimensions in mm (tolerance : +/- 0.2 mm)

Suggested Pad Layout



Physical dimensions in mm (tolerance : +/- 0.2 mm)

Marking information



XX	Product identification code
Y	Year: [0-9]
W	Week: A-Z: [1-29], a-z: [27-52], z=52 and 53
X	Internal code

Ordering Information

Product Name	Ordering Reference	Package	Marking
CXT-741G57	CXT-741G57A-SOT-23-6	SOT-23-6	AA
CXT-741G58	CXT-741G58A-SOT-23-6	SOT-23-6	AC
CXT-741G97	CXT-741G97A-SOT-23-6	SOT-23-6	AB
CXT-741G175	CXT-741G175A-SOT-23-6	SOT-23-6	AD

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