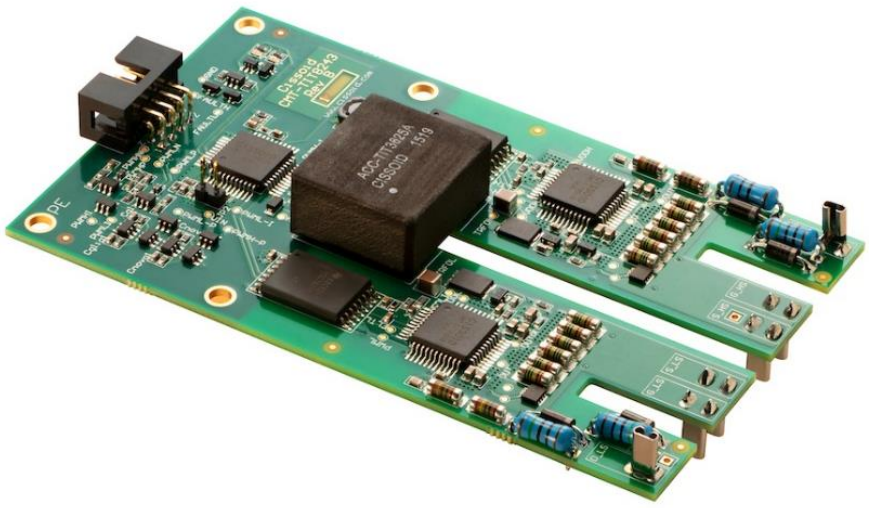
1200V/1700V High Temperature (125°C) Half-Bridge SiC MOSFET Gate Driver Datasheet

Version: 1.6
20-Dec-23
(Last Modification Date)

Features

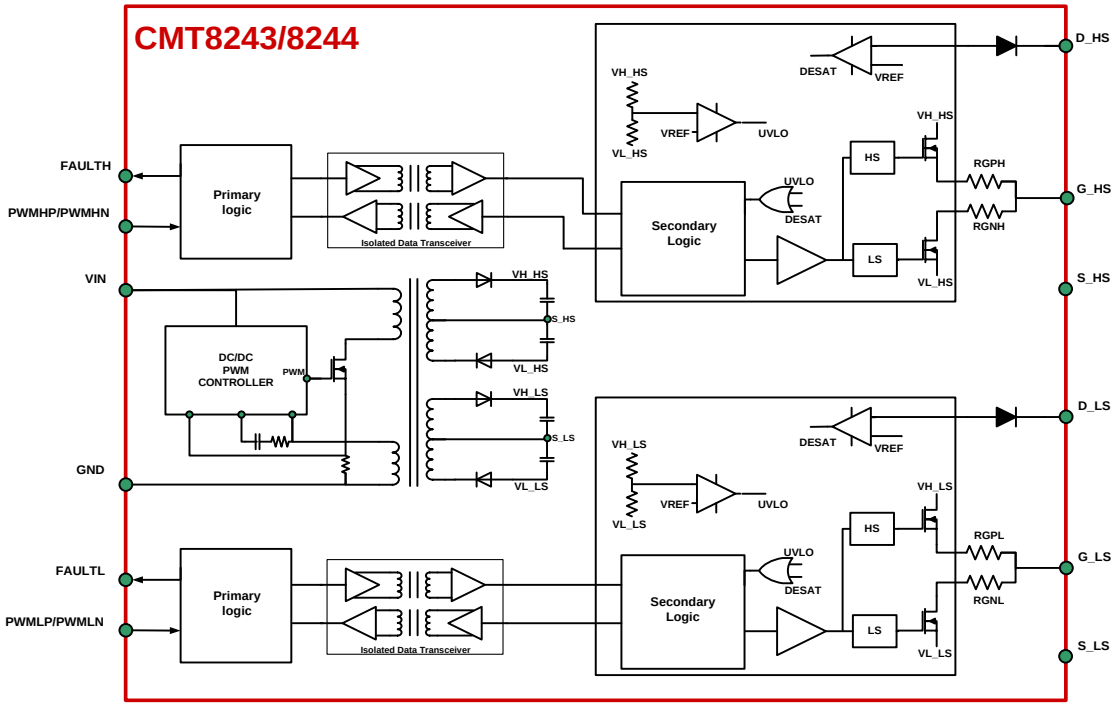
- Designed to drive 62mm 300A SiC MOSFET Power Modules
- Board size: 69 mm * 116 mm
- Operating temperature: -40°C to 125°C
- Bus voltage:1200V/1700V max
- Isolation: 3600VAC @50Hz (1min)
- 14mm Creepage/12mm clearance
- > 50kV/µs dV/dt immunity
- Low parasitic capacitance between primary and high-side: 10pF
- Switching frequency up to 100kHz
- Delay (PWM to VOUT): 200ns typ.
- FET Gate rise/fall time:40ns typ.
- Gate driving voltages: +20V/-5V (3% precision)
- Low inductance gate loop design
- Single power supply: 12V-18V
- RS422 PWM input interface
- Open-drain fault output
- Under voltage lockout (UVLO)
- On-board optional non-overlap generation (via jumper)
- Anti-overlap protection (on PWM inputs)
- Glitch suppressor on PWM inputs
- Active Miller Clamping (AMC)
- Desaturation protection
- Gate-Source short-circuit protection



Ordering Information

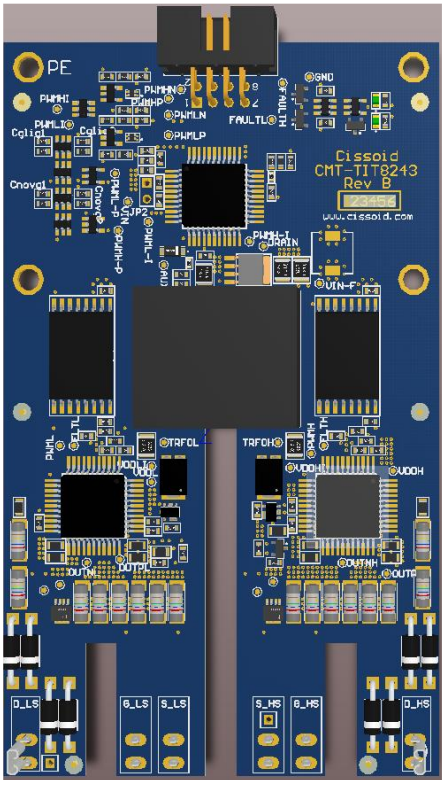
Product Name	Ordering Reference	Voltage	Marking
CMT-TIT8243	CMT-TIT8243A	1200V	CMT-TIT8243A
CMT-TIT8244	CMT-TIT8244A	1700V	CMT-TIT8244A

High level block diagram



IO Description[1]

Pin Name	Pin ID	Pin Description
PMWLN	1	Negative Low-side PWM control signal
PWMHN	2	Negative High-side PWM control signal
PMWLP	3	Positive Low-side PWM control signal
PWMHP	4	Positive High-side PWM control signal
FAULTL	5	Low-side fault
FAULTH	6	High-side fault
GND	7	Ground
VIN	8	Positive supply
PE		Chassis connection
D_HS		High-side drain sense signal
G_HS		High-side gate signal
S_HS		High-side source sense signal
S_LS		Low-side source sense signal
G_LS		Low-side gate signal
D_LS		Low-side drain sense signal



VIN	**Positive supply** All other power supplies for driving the gate of the FETs are internally generated by the on-board DC-DC converter
GND	**Ground** Reference ground for the supply and the digital IOs.
PWMHP/PWMHN	**Input control signals for the high-side driver** These signals control the state of the high-side FET. When in Local mode (selection by jumper), those signals control both low-side and high-side channels in opposite states with some internally defined non-overlapping delay.
FAULTH	**High-side channel fault output (open drain)** This signal combines: - The high-side secondary Desaturation fault - The high-side secondary UVLO fault - The primary fault. In case of fault, FAULTH is set to “0V” for a duration equal to internal timer defined at board level.
PWMLP/PWMLN	**Input control signal for the low-side driver** The signal controls the state of the low-side FET. When in Local mode (selection by jumper), those signals have no effect, the low-side FET being control by PWMH and the local non-overlap function.
FAULTL	**Low-side channel fault output (open drain)** This signal combines: - The low-side secondary Desaturation fault - The low-side secondary UVLO fault - The primary fault. In case of fault, FAULTL is set to “0V” for a duration equal to internal timer defined at board level.
PE	**Chassis connection** A 1000V 1nF capacitance is connected between PE and each of the pins 1 to 8

[1] Refer to section Mechanical characteristics page 13 for more details on connector pinout

Absolute Maximum Ratings

Stressing the board above these absolute maximum ratings could present permanent damage. Exposure to this maximum rating for extended periods may affect the board reliability. These ratings are considered individually (not in combination). If not specified, voltages are related to GND

Parameter	Min.	Max.	Units
(VIN-GND)	-0.5	18	V
Voltage transient on S_HS		100	kV/µs
Voltage on D_HS, D_LS		1200/1700	V
Output power per gate		2.375	W
Steady Operating Temperature (no airflow)	-40	125	°C
Storage Temperature	-40	125	°C

Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold underlined** values indicate values valid over the whole temperature range (-40°C < T_a < +125°C).

Parameter	Condition	Min	Typ	Max	Units
External Power Supply					
External Power Supply VIN	Versus GND	**12**		**18**	V
I_{AVG}(VIN)	VIN=12V, no PWM No fault situation Direct Mode Load: CREE WOLFSPEED-CAS300M12BM2		103		mA
	VIN=12V; 20 kHz; 50% Duty-Cycle No fault situation Direct Mode Load: CREE WOLFSPEED-CAS300M12BM2		220		mA
I_{AVG}(VIN) max	VIN=12V			**500**	mA

Parameter	Condition	Min	Typ	Max	Units
Isolation					
Inter channel Isolation I_{H2L}	S_HS to S_LS (50Hz, 1min)	**3.6**			kVrms
Low-side channel isolation I_{L2P}	S_LS to GND (50Hz, 1min)	**3.6**			kVrms
High-side channel isolation I_{H2P}	S_HS to GND (50Hz, 1min)	**3.6**			kVrms
Maximum supported dV/dt	S_HS to S_LS S_HS to GND (guaranteed by design)	**50**			kV/µs
Parasitic capacitance	Between High-Side and Primary		**10**		pF
Creepage	Primary to any secondary Between secondaries	**14**			mm
Clearance	Primary to any secondary Between secondaries	**12**			mm

Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold underlined** values indicate values valid over the whole temperature range (-40°C < T_a < +125°C).

Parameter	Condition	Min	Typ	Max	Units
PWML/PWMH inputs					
Common mode input level		**-6**		**+10**	V
Differential input high-threshold voltage	Diff(PWMxP,PWMxN)	**200**			mV
Differential input low-threshold voltage	Diff(PWMxP,PWMxN)			**-50**	mV
Differential input impedance			**200**		Ω
Minimum pulse width	Configurable via capacitances Cglil (on PWML) and Cglih (on PWMH)		50		ns
Anti-overlap duration (t_{novp})	Direct Mode Configurable via capacitances Cnovpl (on PWML) and Cnovph (on PWMH)		450		ns
Maximum frequency				**100**	kHz
Duty cycle		**0**		**100**	%
Propagation delay (PWML/PWMH →G_LS/G_HS) (50% to 10%)	Direct Mode Default settings for glitch suppressor and anti-overlap prevention		170		ns
Non-overlap duration[2]	Local Mode (configurable via capacitance Cnovd)		480		ns
FAULTL/FAULTH open drain outputs					
On resistance	Applies to **FAULTL/FAULTH**			**25**	Ω
Fault local latching time (at Primary or at Secondary)			14		ms

Parameter	Condition	Min	Typ	Max	Units
G_LS/G_HS Gate driver outputs					
High level		**19.4**	20	**20.6**	V
Low level		**-5.2**	-5	**-4.8**	V
Maximum average output load current				**95**	mA
Peak output current	Rgate_on=Rgate_off= 0Ω	**10**			A
Rgate_on			1.8		Ω
Rgate_off			1.8		Ω
Gate-Source resistance			100		kΩ
Active Miller Clamp (AMC) transistor R_{dson}			33		mΩ
D_LS/D_HS Desaturation Monitoring inputs					
Voltage range	CMT8243	**0**		**1200**	V
	CMT8244	**0**		**1700**	V

Parameter	Condition	Min	Typ	Max	Units
Under-voltage Lockout on primary supply (VIN) (UVLO_P)					
UVLO_P High Threshold			9.75		V
UVLO_P Low Threshold			8.2		V
Under-voltage Lockout on secondary supplies (VDD_L-VSS_L)/ (VDD_H-VSS_H) (UVLO_S)					
UVLO_S High Threshold			22.7		V
UVLO_S Low Threshold			20.5		V
Desaturation detection					
Threshold on D_LS/D_HS	D_LS/D_HS wrt to S_LS/S_HS (configurable via resistance Rdesatx)		4.34		V
Desaturation Blanking time	Configurable via capacitance Cdesatdx (68pF Cdesatdx installed)		1		µs
Delay from desaturation detection to G_LS/G_HS starting to turn off			350		ns
G_LS/G_HS turn-off time after desaturation detection	From 20V to 0V Load : CREE WOLFSPEED-CAS300M12BM2		1		µs
Soft Shutdown (SSD) resistor			20		Ω
Start-up					
Start-up time			30		ms

[2] Non-overlap delay includes glitch suppressor delay; 10pF parasitic capacitance to be added to Cnovd

Circuit Functionality

Description

CMT-TIT8243/8244 board is a Half-Bridge gate driver board meant to drive 62mm SiC power modules (typically CREE WOLFSPEED CAS300M12BM2).

Its main features are:

- Isolated data transmission (robust to high dV/dt) (data and fault) on both high and low side channels
- Adjustable fault timer with automatic restart
- Safe start-up sequence through monitoring of the main supply (UVLO) and of the voltage regulators output (through Power-Good function)
- Permanent and programmable Under-Voltage Lockout (UVLO) monitoring on external and internally generated power switch supplies
- Desaturation detection function with programmable blanking time and threshold protecting power switches in case of abnormal current levels
- Soft-Shutdown transistor and control performing power device graceful shutdown in case of fault and so preventing too high dI/dt in the power stage
- Active Miller Clamping (AMC)
- Flyback DC-DC convertor with cycle-by-cycle current limit for short circuit protection
- High-precision (typ 3%) high-level gate voltage generation
- Differential RS422 PWM inputs
- Open-drain low-ohmic (typ. 25Ω) FAULT output
- Support of 2 separate incoming PWM channels and of locally generated non-overlapped PWM signals
- Configurable 50ns (typ) spike filter on incoming PWM signal for enhanced noise robustness
- Configurable 200ns (typ) anti-overlap protection on incoming PWM signals
- Gate-2-Source short-circuit protection

Under-Voltage Lockout (UVLO)

CMT-TIT8243/8244 board monitors constantly:

- VIN power supply
- High-side secondary supplies (typ +20V/-5V)
- Low-side secondary supplies (typ +20V/-5V)

At primary side, the monitored power supply is “VIN-GND”; to avoid oscillation when (VIN-GND) is close to the UVLO threshold, a hysteresis is implemented.

At each secondary side, the monitored power supply is “VDD_L-VSS_L”/ “VDD_H-VSS_H”; to avoid oscillation when (VDD_x-VSS_x) is close to the UVLO threshold, a hysteresis is implemented.

Refer to the chapter Fault Management/LED status for details about fault behavior and management.

On-board power supplies

The on-board isolated power supply is a regulated flyback DC-DC converter providing both channels with the positive and negative supply voltages required to drive the power FETs. It offers high voltage isolation between the channels, high dV/dt sustainability and very low parasitic capacitance. Cycle-by-cycle current monitoring at primary side is implemented to protect the board against short-circuit.

High accuracy (typ 3%) is achieved on all secondary positive supplies.

Interface towards controller

PWM inputs

PWML and PWMH input interface is based on RS422 differential receivers to increase noise immunity on those incoming signals. Are high impedance inputs.

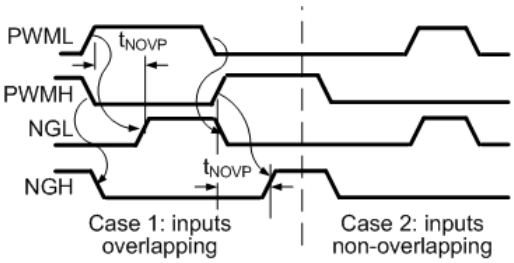
CMT-TIT8243/8244 board implements 2 protection functions on the PWM data paths:

- **Anti-glitch**: any negative or positive glitch on PWML/PMWH signals smaller than a programmed value is ignored by the board; this is increasing immunity of incoming signals against external noise; the signals are delayed by the corresponding anti-glitch time

$$t_{MINPW}\ (ns) = 0.5 * [C_{GLIx}\ (pF)]$$

- **Anti-overlap**: this circuit prevents PWML and PMWH to be active at the same time by forcing an internal non-overlap time; if PWML and PWMH are not overlapping by more than the internally programmed time, they are not delayed internally. If PWML and PWMH are active for a long period, both gate outputs are forced to zero until one of the inputs goes to zero.

$$t_{NOVP}\ (ns) = 0.5 * [C_{NOVPx}\ (pF)]$$



FAULT outputs

The output buffers operate as an open-drain driver with a low Ron resistance (typ. 25Ω), enabling the use of low value pull-up resistance for increased noise immunity.

Isolated data transmission

CMT-TIT8243/8244 board uses integrated digital isolators. Those devices provide isolation, immunity against high dV/dt and low parasitic capacitance.
In case no power supply is present at the secondary side, a fault is generated at the primary side.

Desaturation detection

The purpose of the desaturation function is to detect that the voltage at the drain of the power switch, in “ON” state, is higher than a given threshold. This informs the logic part of the system about possible damage of the power arm (e.g. a short circuit at the arm level leading to an over-current in the power switch).
The sensing of the power device drain voltage is performed through a high voltage sensing diode whom cathode is connected to the power switch drain and whom anode is connected to a current source (typ 2mA) and a sensing circuit.

The desaturation threshold (on D_LS/D_HS nodes) is configured by on-board resistors and can be tuned according to the table below.

Rdesat value	Desat threshold (V)	
	25°C	125°C
0KΩ	0.93	1.22
5KΩ	2.35	2.62
10KΩ (default)	3.77	4.02
15KΩ	5.18	5.42
20KΩ	6.6	6.82
30KΩ	9.42	9.62

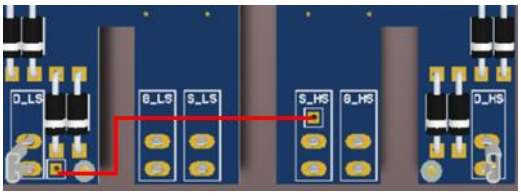
At system level, the de-saturation detection should only be taken into account after a defined time following the low-to-high transition on the power device gate. This “blanking” time t_{DESAT_D} is implemented and adjusted by an on-board capacitor C_{DESATD} (68pF installed) and can be calculated as follows:

$$t_{DESATD}\ (ns) = 14 * [C_{DESATD}\ (pF) + 7]$$

If after t_{DESAT_D} time, the DESAT comparator output indicates that D_LS/D_LS level is higher than the programmed threshold value, an internal DESAT fault is generated. Refer to the chapter Fault Management/LED status for details about fault behavior and management.
When the desaturation fault is detected, the power module gate is gracefully discharged thanks to the Soft-Shutdown circuit to avoid high dI/dt at power module turn-off

To sense the drain voltage, fast-on connectors are present on the board (see them marked D_HS, D_LS on picture below). For D_LS signal sensing, instead of a wire towards the power module, a wire

between D_LS net and S_HS net (see wire in red on picture below) can be added by the customer; this can simplify the wiring towards the power module.



Active Miller Clamping

In case of high positive dV/dt and despite the negative drive of the power module gate, a parasitic turn-on of the gate could take place, inducing shoot-through current on the power arm.
To prevent this, CMT-TIT8243/8244 board implements an Active Miller Clamping function by bypassing the gate resistance with a low ohmic path (implemented with a transistor) when the gate is driven negative.
This transistor also helps to limit the amplitude of negative kick on the power module gate in case of negative dV/dt.

Fault Management/LED status

At primary side, fault is generated by any of those situations:

- Main power supply (VIN) is below the UVLO threshold
- Primary linear voltage regulator (generating the 5V output required by the on-board logic) is below the internal Power Good level

Those faults are internally combined to generate a unique fault signal. This internal fault signal is latched for 14msec.

While the fault is latched:

- Both FAULTL/FAULTH pins are tied to “0”
- Both power switches are turned off
- On board DC-DC converter is off

After the predefined latch time period, CMT-TIT8243/8244 board will attempt to return to normal operation:

- If the fault is still present, CMT-TIT8243/8244 board will stay in the fault state till the fault disappears
- If the fault disappeared (e.g. temporary UVLO situation), CMT-TIT8243/8244 board will go out of FAULT state and return to normal operation (DC-DC converter turned on and data paths active); still, on the PWM path, transition to normal operation will happen on the next positive edge of the incoming PWM signal.

The primary fault state is combined with the faults returned by the secondary devices according to Table 1.

Prim fault	Low-side fault	High-side fault	FAULTL	FAULTH
No	No	No	No fault	No fault
No	Yes	No	Fault	No fault
No	No	Yes	No fault	Fault
No	Yes	Yes	Fault	Fault
Yes	Yes or No	Yes or No	Fault	Fault

Table 1: FAULT aggregation table

At each of the secondary side, fault is generated by any of those situations:

- Power supply is below the UVLO threshold
- Secondary voltage regulator (5V) output voltage is below the Power-Good threshold
- Desaturation situation is detected by the DESAT comparator

Those faults are internally combined to generate a unique fault signal. This internal fault signal is latched for 14msec.
While the fault is latched, the gate driver is turned off. At the transition between “no fault” and “fault” situation, the gate driver circuit is gracefully shut down (Soft Shut-Down).

After the predefined latch time period, the gate driver circuit returns to normal operation:

- If the fault is still present, the gate driver is kept turned off till the fault disappears
- If the fault disappeared (e.g. temporary UVLO situation), normal operation will resume on the next positive edge of incoming PWM signal

2 LEDs are present on the CMT-TIT8243/8244 board and are reflecting board status as follows:

State	LED1		LED2	
	State	Color	State	Color
No supply	Off	None	Off	None
Operational	On	Green	Off	None
Primary or secondary fault	On	Green	On	Red

Modes of operation

CMT-TIT8243/8244 board offers 3 modes of operation:

- Direct Mode: PWML and PWMH are generated independently outside CMT-TIT8243/8244 board. In this case, proper non overlapping must be generated externally. Glitch filter is active on both PWM incoming signals
- Local Mode: PWML and PWMH are generated out of one input signal (PWMH) and proper non overlapping timing is managed locally on the CMT-TIT8243/8244 board (cfr Figure 1). Glitch filter is active on PWMH signal. In this mode, at board start-up, both gate signals are inactive. However, when PWMH is low, low-side gate is “high” while high-side gate is “low”.

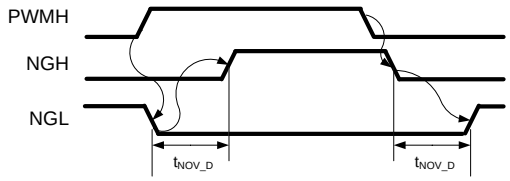
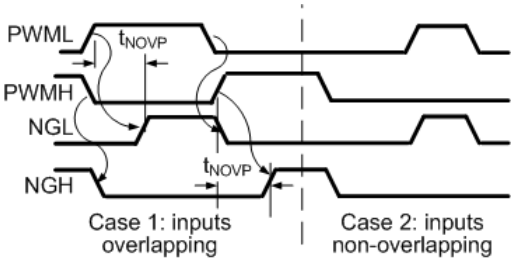


Figure 1: Local Mode operation

- Use of anti-overlap function
  The drawback of using the Local Mode is that it is not possible to force the 2 gate signals to “low”.
  When using the board in Direct Mode and applying PWMH and PWML being exactly the opposite of each other, the board will generate 2 gate signals which are non-overlapped by a time equal to t_{novp} (see figure below) but when forcing the 2 PWM signals to “low”, the 2 gates signals will be forced to “low”.



The choice between Direct and Local modes of operation is made via the jumper JP1.

When in Local Mode, an on-board capacitance (Cnovd) defines the non-overlap delay according to following formula:

$$t_{NOV\_D}\,(\mathrm{ns}) = 5.5 * C_{NOVD}(\mathrm{pF})$$

Board power dissipation

Current consumption of the CMT-TIT8243/8244 board (Vin=12V) can be computed as follows:

$$Iin = 103mA_{typ} + Act * (0.26 + 0.0055 * Qg) * Fs$$

Where:

- Iin is the input current (in mA) (wrt to Vin = 12V)
- Act is a Boolean (0: PWML/PWMH = 0, 1: PWM_L/PWM_H alternating at Fs frequency)
- Gg: Total gate charge of one power transistor (in nC)
- Fs: Switching frequency (in kHz)

The duty cycle of the PWML/PWMH signals has almost no influence on the current consumption of the CMT-TIT8243/8244 board (assuming PWML and PWMH duty cycles are complementary).

To stay within specifications of the internal secondary voltages, the maximum average Iin current should be 500 mA (for Vin =12V).

Dynamic behavior

Figure 2 illustrates the CMT-TIT8243/8244 low-side driver dynamic behavior in normal operation and fault conditions.

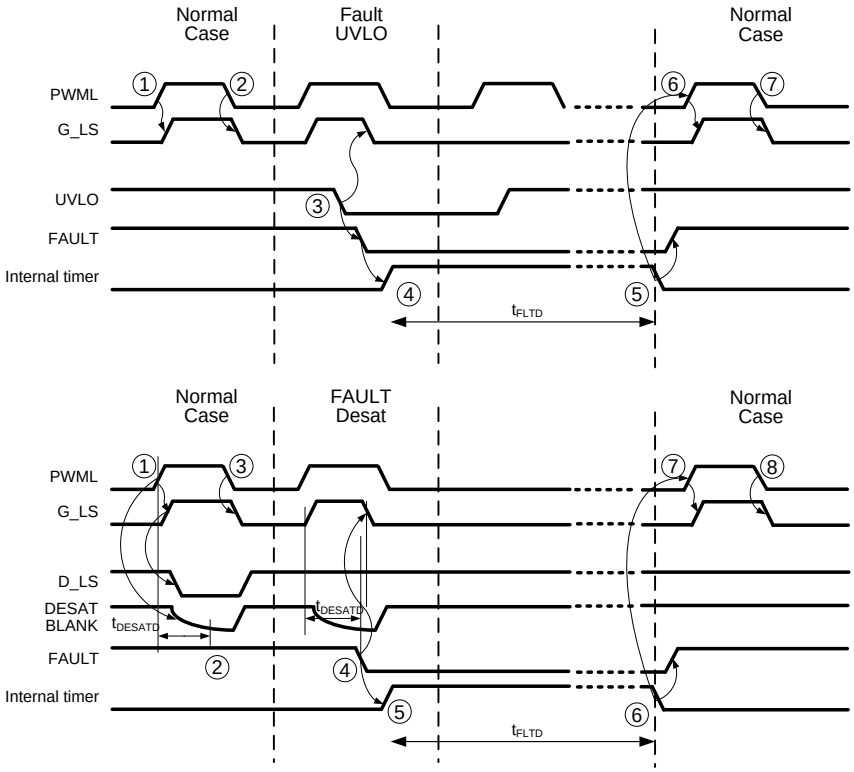


Figure 2: Timing diagram CMT-TIT8243/8244 low-side driver behaviour

In Normal operation

on PWML rising edge (1), rising edge is generated on G_LS (after propagation delay through CMT-TIT8243/8244 board).
After rising edge on G_LS, low-side power module is turned ON and midpoint node is going to "0" state (voltage equals to Ron * current flowing through the power device). D_LS node is also pulled down and after blanking time (t_{DESAT_D}), no desaturation fault is detected and FAULTL remains high.

On PWML falling edge (2), falling edge is generated on G_LS (after propagation delay through CMT-TIT8243/8244 board)
After falling edge on G_LS, the low-side power device is turned OFF.

In DESAT fault situation

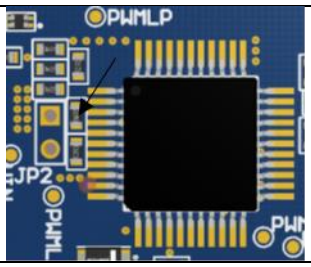
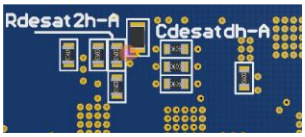
on PWML rising edge (3), rising edge is generated on G_LS (after propagation delay through CMT-TIT8243/8244 board)

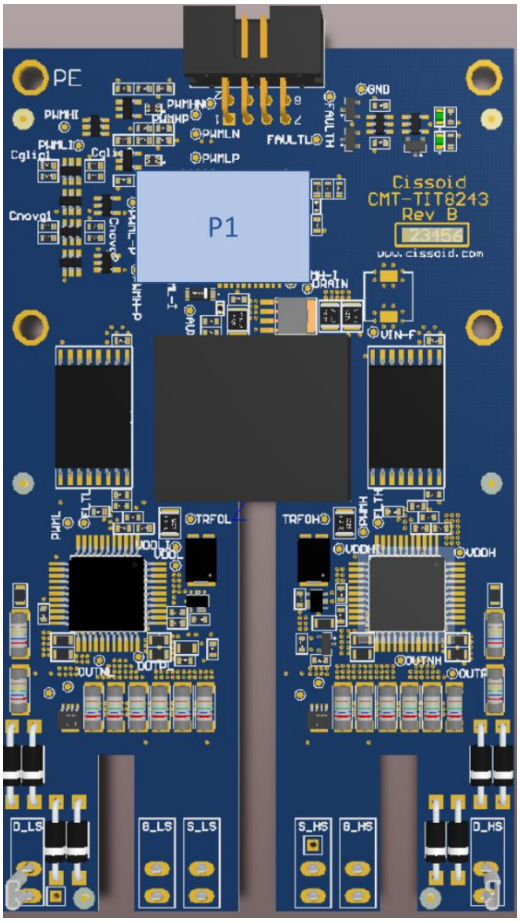
After rising edge on G_LS, low-side power module is turned ON; because of a desaturation fault, D_LS node does not reach its normal "0" level. Thanks to the DESAT comparator, CMT-TIT8243/8244 board detects this fault situation and turns off gracefully G_LS. Power device is turned off. FAULTL signal is pulled down. Fault is cleared after fault timer expiry.

In UVLO fault situation

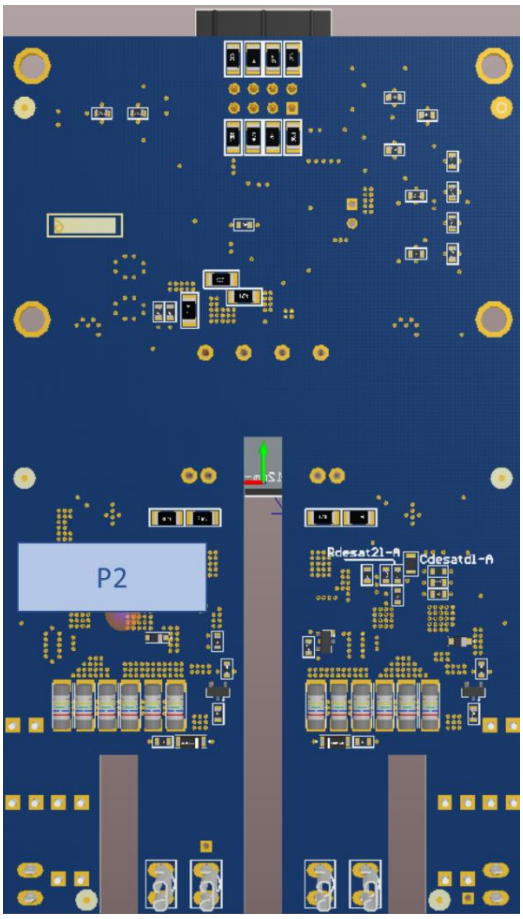
UVLO status is monitored inside the secondary devices (and inside primary device as well; for clarity, only secondary UVLO situation is described here). When UVLO comparator (5) detects an under-voltage situation, G_LS is gracefully shut down FAULTL signal is pulled down. Fault is cleared after fault timer expiry.

Settings Management

Function	Position on PCB	Component name	Component location	Settings
Direct/Local Mode	P1	JP2 (top)		Jumper not present: Direct mode Jumper present: Local mode
Non-overlap time		Cnovd (top)		t_{NOV_D} (ns)=5.5 * C_{NOVD}(pF)
Desaturation threshold	P2	Rdesat2h-A		Cfr section Desaturation de-tection
Desaturation blanking time		Cdesath-A		

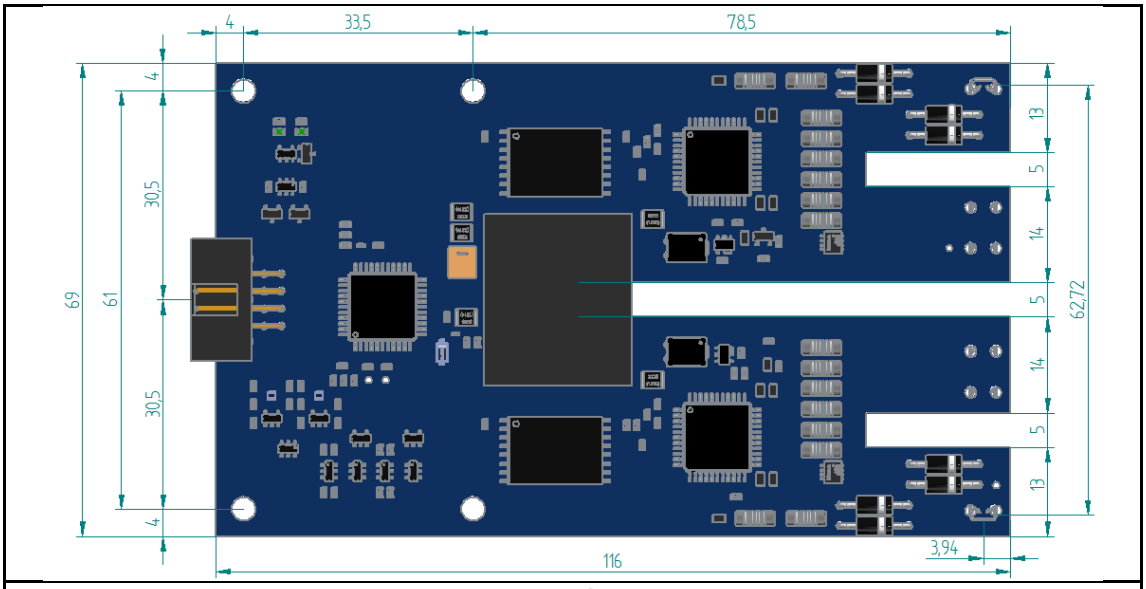


Top view

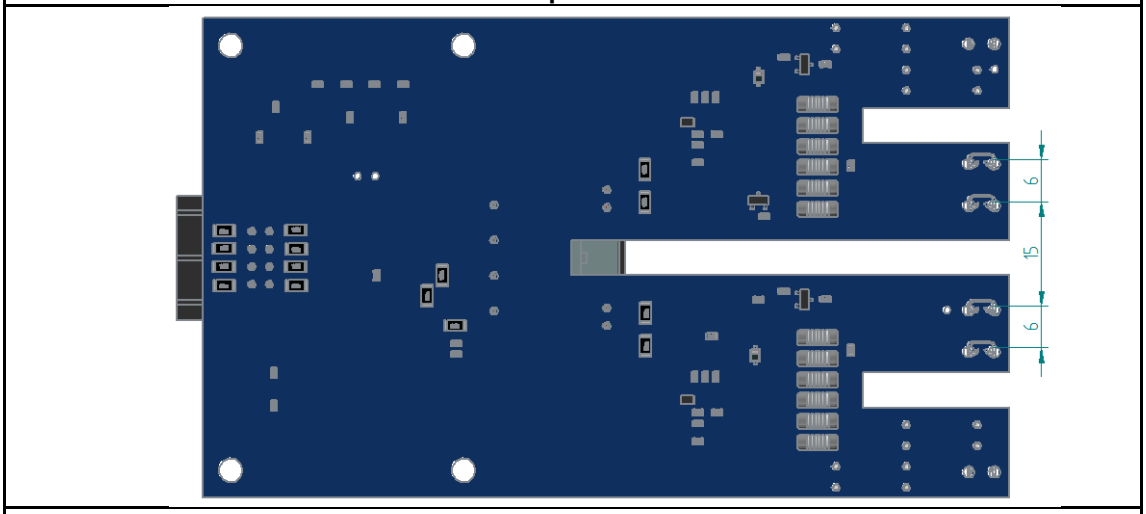


Bottom view

Mechanical characteristics

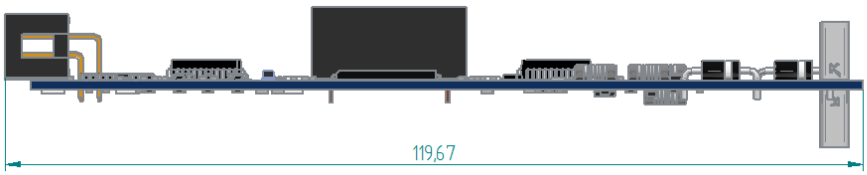


Top view

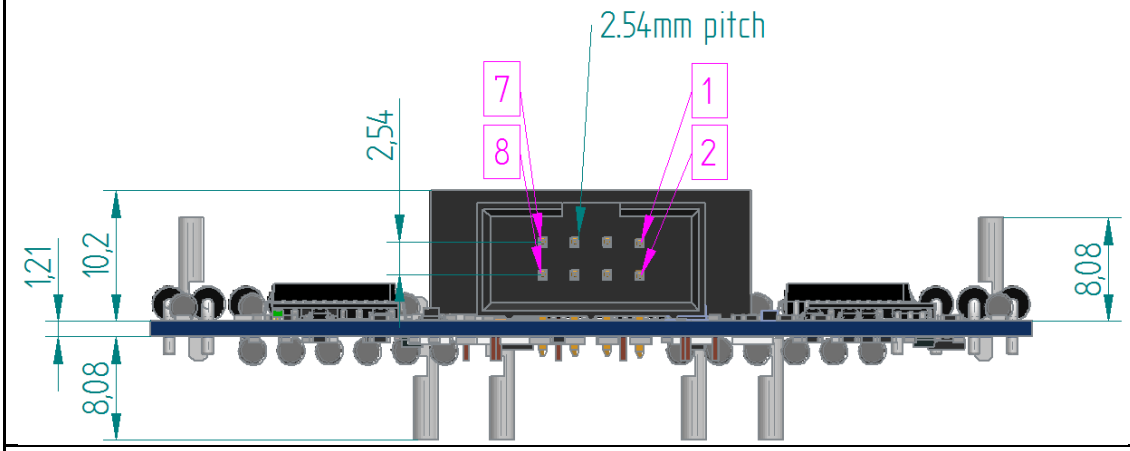


Bottom view

Mechanical characteristics (cnt'd)



Side view



Front view

Contact

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