CMT-PLA9869
Datasheet

Version: 1.1
14-Dec-23
(Last Modification Date)

1200V/40mOhm SiC MOSFET

General description

CMT-PLA9869 is a High Temperature, High Voltage, Silicon Carbide (SiC) MOSFET transistor, available in standard TO-247 package. The product is guaranteed for normal operation over the full range -55°C to +175°C (Tj). The device has a break-down voltage in excess of 1200V and can switch currents up to 60A. The device features a body diode that can be used as free-wheeling diode.

Features

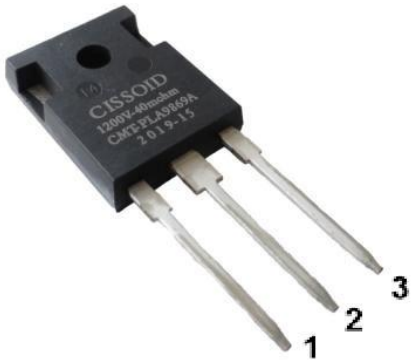
- Specified from -55 to +175°C (Tj)
- V_{DS} Max: 1200V
- I_{DS} @ 25°C: 60 A
- $R_{DS(on)}$: 40mΩ typ
- Low Switching Energy
  - Eon= 1mJ
  - Eoff= 0.4mJ
- Voltage control: V_{GS}=-4V/18V
- Gate charge: Q_{GS}=32nC
- Low capacitance: C_{OSS}=181 pF
- Package: TO-247 (MSL3)
- Thermal Safe Operation Area model
- RoHS Compliant

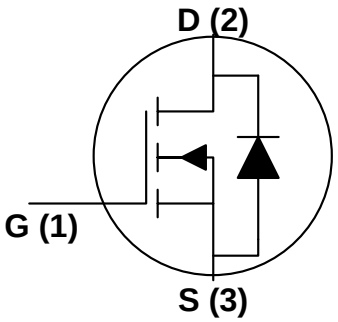
Benefits

- Increased System Switching Frequency
- Higher System Efficiency
- Reduced Cooling Requirements
- Increased Power Density
- Seamless driving with HADES® gate driver solutions

Applications

- Switched-mode Power Supplies
- High Voltage DC-DC converters
- Motor Drives
- Battery Chargers
- Solar Inverters





Absolute Maximum Ratings

Unless otherwise stated, T_j =25°C. **Bold** figures point out values valid over the whole temperature range (T_j =-55°C to +175°C).

Symbol	Parameter	Value	Unit	Test conditions	Note
V_{DSmax}	Drain-Source Voltage	1200	V	VGS=0V, ID=100µA	
V_{GSmax}	Gate-Source Voltage	-10/20	V	Absolute maximum values	
V_{GSop}	Gate-Source Voltage	-4/18	V	Recommended operational values	
I_D	Continuous Drain Current	60	A	VGS=20V, T_C=25°C	
		40		VGS=20V, T_C=100°C	
$I_{D(pulse)}$	Pulsed Drain Current	160	A	Pulse width t_P limited by T_{jmax}	
P_D	Power Dissipation	330	W	T_C=25°C, T_J=150°C	
T_J,T_{stg}	Operating Junction and Storage Temperature	-55 to + 175	°C		
T_L	Solder Temperature	260	°C	1.6mm from case for 10s	
M_d	Mounting Torque	1	Nm	M3	

Electrical characteristics

Unless otherwise stated, T_j =25°C. **Bold** figures point out values valid over the whole temperature range (T_j =-55°C to +175°C).

Symbol	Parameter	Min	Typ	Max	Unit	Test conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	**1200**			V	V_{GS}=-4V, I_D=100µA	
$V_{GS(th)}$	Gate Threshold Voltage		2.35		V	V_{DS}= V_{GS}, I_D=10mA	
			1.67		V	V_{DS}= V_{GS}, I_D=10mA, T_J=175°C	
I_{DSS}	Zero Gate Voltage Drain Current		5		µA	V_{DS}=1200V, V_{GS}=0V	
I_{GSS}	Gate-Source Leakage Current		10	100	nA	V_{GS}=18V, V_{DS}=0V	
$R_{DS(on)}$	Drain-Source On-State Resistance		40		mΩ	V_{GS}=18V, I_{DS}=40A	
			73		mΩ	V_{GS}=18V, I_{DS}=40A, T_J=175°C	
g_{fs}	Transconductance		18		S	V_{DS}=10V, I_{DS}=40A	
			17.6			V_{DS}=10V, I_{DS}=40A, T_J=175°C	
C_{iss}	Input capacitance		3367		pF	V_{GS}=0V V_{DS}=600V F=1MHz V_{AC}=25mV	
C_{oss}	Output capacitance		181				
C_{rss}	Reverse Transfer capacitance		32				
E_{oss}	Coss Stored Energy		32		µJ		
E_{ON}	Turn-On Switching Energy		1		mJ	V_{DS}=600V, V_{GS}=-4V/18V, I_D=40A, $R_{G(ext)}$= 3Ω, L=50µH	
E_{OFF}	Turn-Off Switching Energy		0.4		mJ		
$t_{d(on)}$	Turn-On Delay Time		18		ns	V_{DS}=600V, V_{GS}=-4V/18V, I_D=20A, $R_{G(ext)}$= 3Ω, L=400µH Per IEC60747-8-4 pg 83	
t_r	Rise Time		55				
$t_{d(off)}$	Turn-Off Delay Time		30				
t_f	Fall-Time		36				
$R_{G(int)}$	Internal Gate Resistance		5		Ω	F=1MHz, V_{AC}=25mV	
Q_{gs}	Gate to Source Charge		32		nC	V_{DS}=600V, V_{GS}=-4V/18V, I_D=20A, Per IEC60747-8-4 pg 21	
Q_{gd}	Gate to Drain Charge		36				
Qg	Total Gate Charge		163				

Reverse Diode Characteristics

Unless otherwise stated, T_j =25°C. **Bold** figures point out values valid over the whole temperature range (T_j =-55°C to +175°C). Timing definitions according to JEDEC 24 page 27

Symbol	Parameter	Min	Typ	Max	Unit	Test conditions	Note
V_{SD}	Diode Forward Voltage		5.2		V	V_{GS}=-5V, I_{SD}=20A, T_J=25°C	
			4.4		V	V_{GS}=-5V, I_{SD}=20A, T_J=175°C	
I_S	Continuous Diode Forward Current		60		A	T_C=25°C	
t_{rr}	Reverse Recovery Time		27		ns	V_{GS}=-5V, I_{SD}=40A T_J=25°C, V_R=600V dif/dt=2500A/µs	
Q_{rr}	Reverse Recovery Charge		170		nC		
I_{rr}	Peak Reverse Recovery Current		9.6		A		

Thermal Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test conditions	Note
$R_{\theta JC}$	Thermal Resistance Junction to Case		0.33	0.38	°C/W		

Typical Performance Characteristics

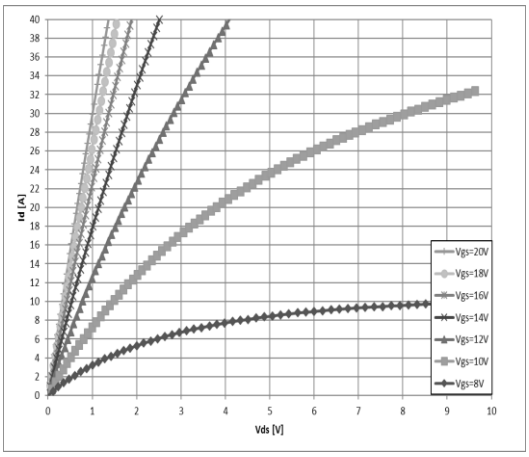


Figure 1: Drain current vs V_{DS} (T_j=-40°C)

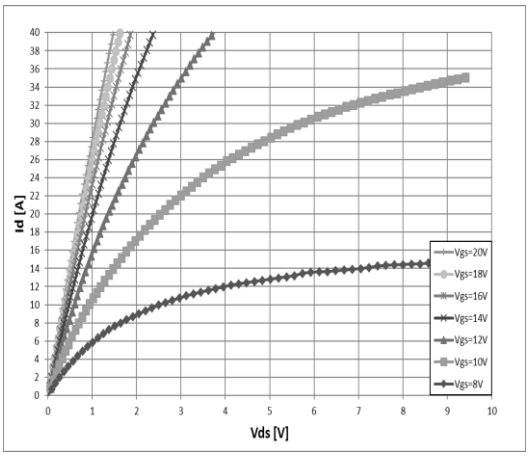


Figure 2: Drain current vs V_{DS} (T_j=25°C)

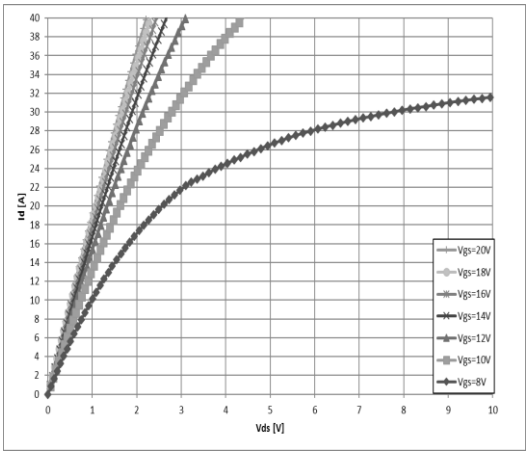


Figure 3: Drain current vs V_{DS} (T_j=125°C)

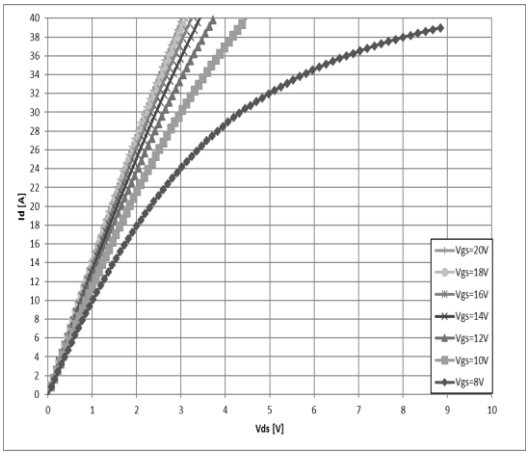


Figure 4: Drain current vs V_{DS} (T_j=175°C)

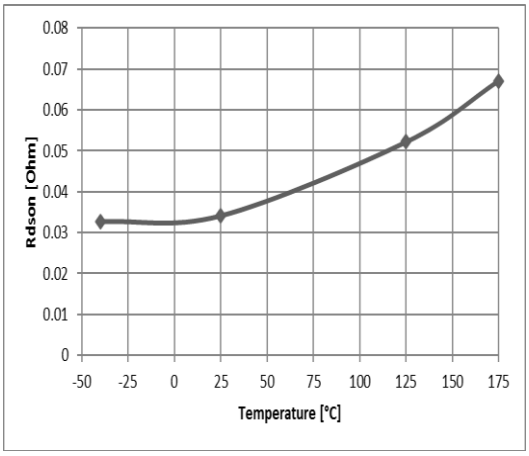


Figure 5: On-state drain source resistance vs. Temperature (V_{GS} =20V; I_{DS}=10A)

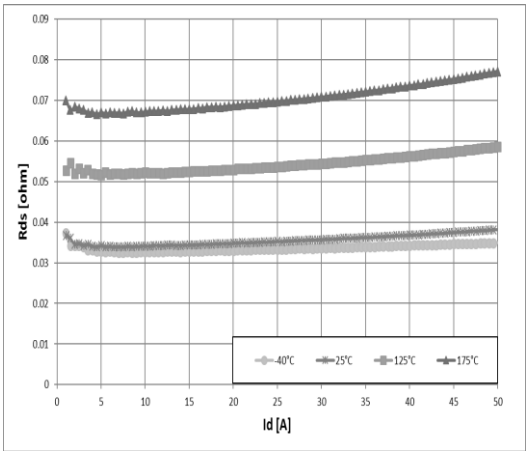


Figure 6: On-state drain source resistance vs. Drain current and temperature (V_{GS} =20V)

Typical Performance Characteristics (cnt'd)

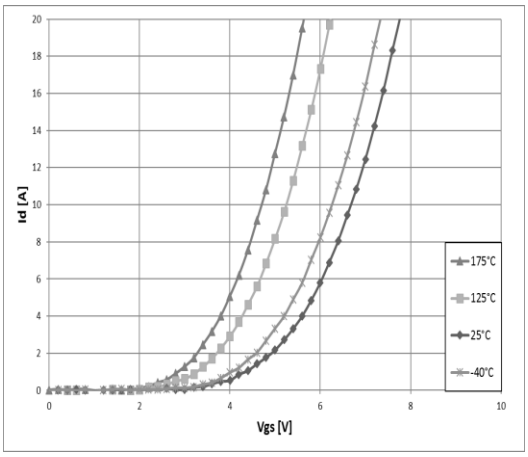


Figure 7: Drain current vs V_{GS} (V_{DS}= 10V)

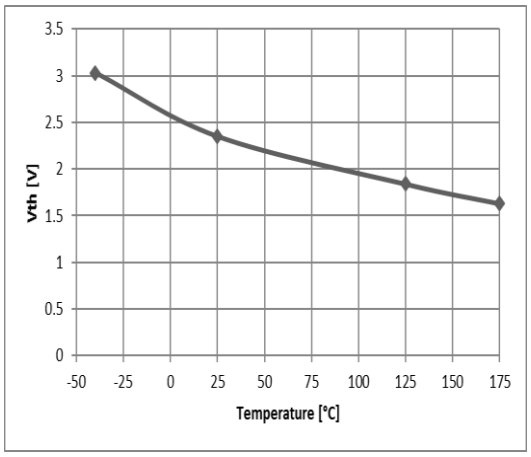


Figure 8: Threshold voltage vs temperature

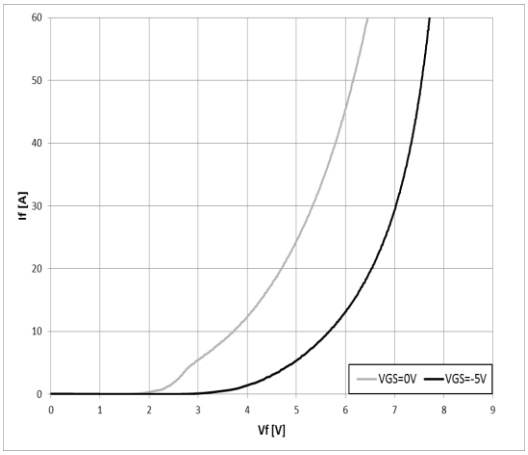


Figure 9: Body diode I_F vs V_F at -55°C

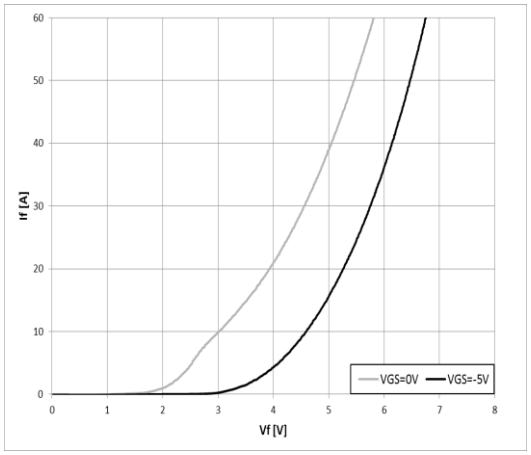


Figure 10: Body diode I_F vs V_F at 25°C

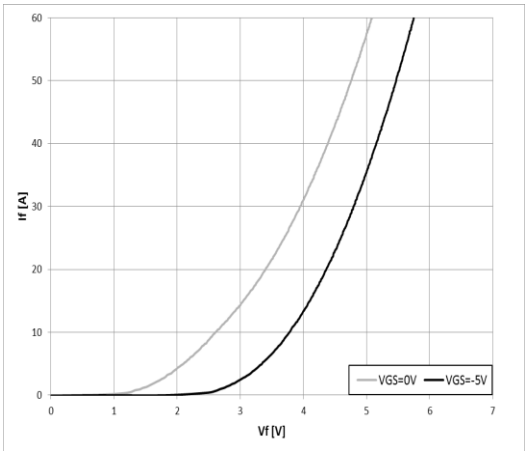


Figure 11: Body diode I_F vs V_F at 175°C

Typical Performance Characteristics (cnt'd)

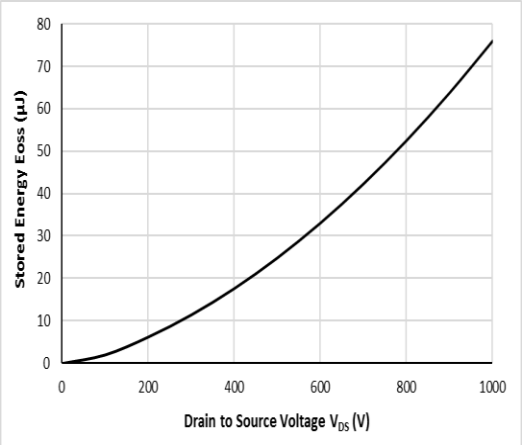


Figure 12:Output Capacitor Stored Energy

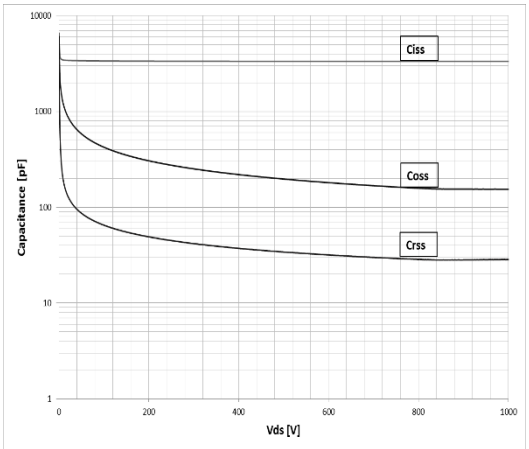


Figure 13:Capacitances vs V_{DS} (T_j=25°C)

Typical Performance Characteristics (cnt'd)

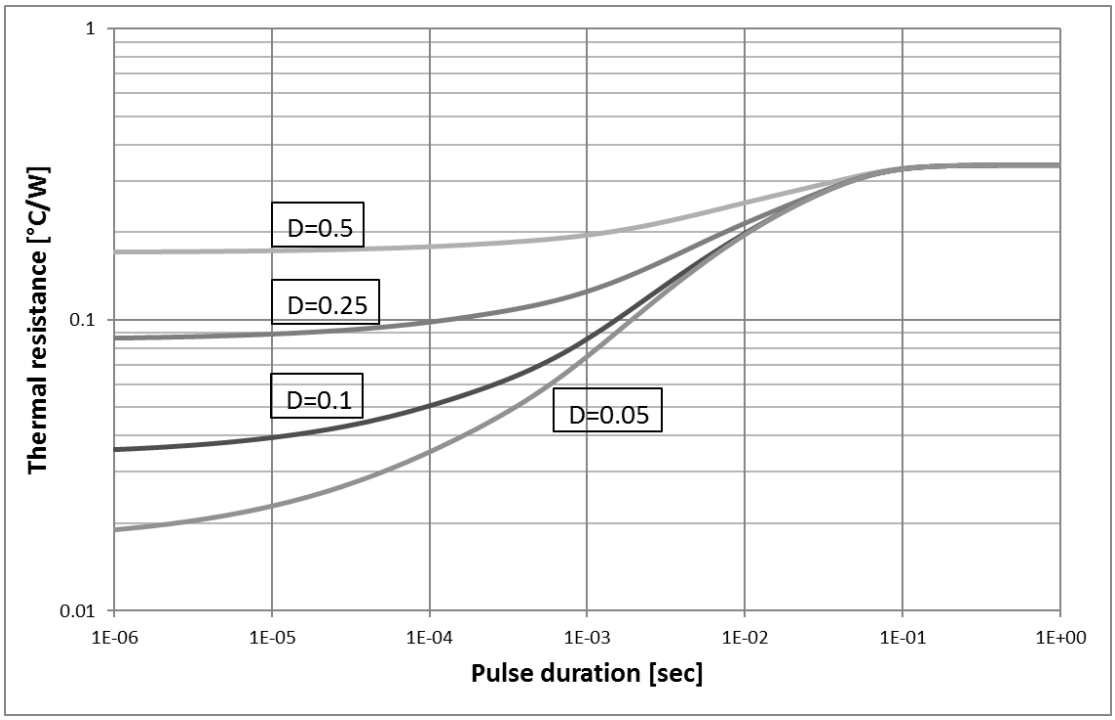


Figure 14: Transient thermal resistance

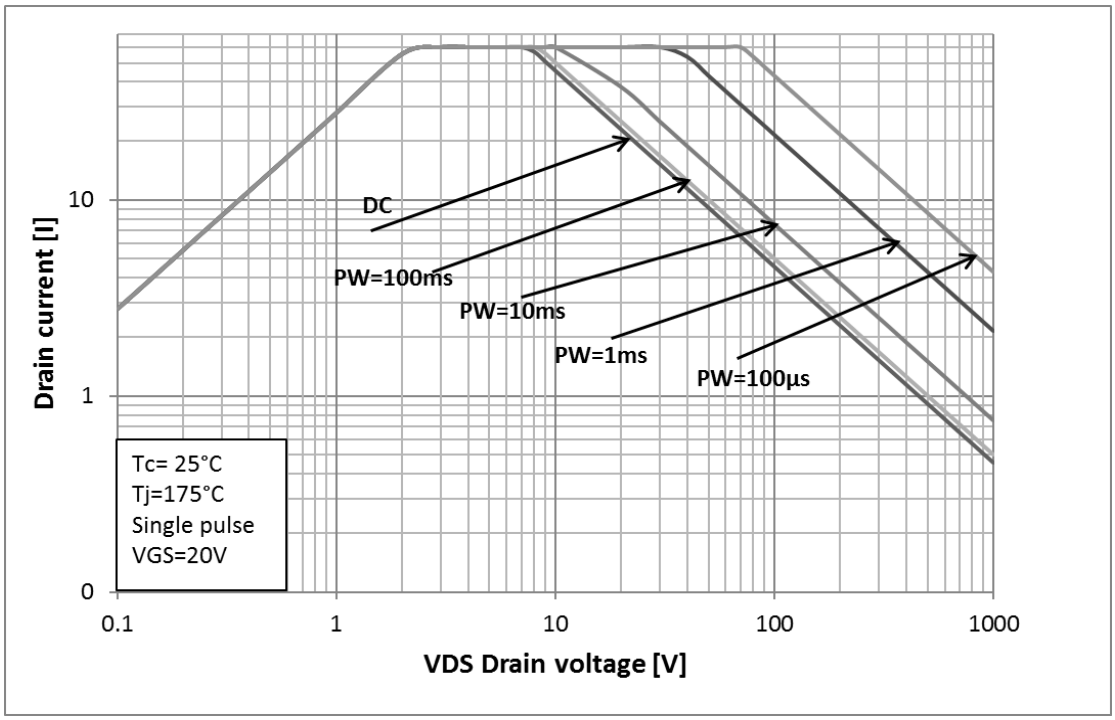


Figure 15: Safe Operating Area

Thermal Safe Operating Area

In power electronics, thermal design is an essential part of the design process. CMT-PLA9869 device junction-to-case thermal resistance, R_{thJ-C} is very low (0.33°C/W). However, when designing the system, one needs to consider the end-to-end junction-to-air thermal resistance which can be evaluated using FEA tools or physical measurements. With too high a thermal resistance, it is possible that any power device will experience thermal runaway. This situation should of course be avoided as it leads to the device destruction.

The graph below will help system designers to dimension their system properly. Firstly, it plots the device resistive losses as a function of temperature for different DC currents. Since Rdson increases with temperature, power dissipation increases with temperature as well. The curves do not include the dissipation due to switching losses which tends to be quite flat over the entire temperature range so therefore an offset may be applied to the curves to take it into account.
Secondly, it plots (in dotted lines) the behavior of the thermal system: the room temperature (point crossing the X-axis at zero power) at which the system operates (e.g. Ta=90°C in the graph example below) and the global junction-to-air thermal resistance (the slope of the straight lines).
To have a stable and healthy system, one needs to ensure that the dotted line (corresponding to the designed thermal system) and the relevant (function of the DC current flowing through the device) power dissipation line are crossing each other at a temperature point below the recommended maximum junction operating point of the device.

As examples:

- With a system thermal resistance of 3°C/W, using CMT-PLA9869 with any DC current above 20A will lead a junction temperature outside of the recommended conditions.
- With a system thermal resistance of 1°C/W, up to 35A DC current can be used.

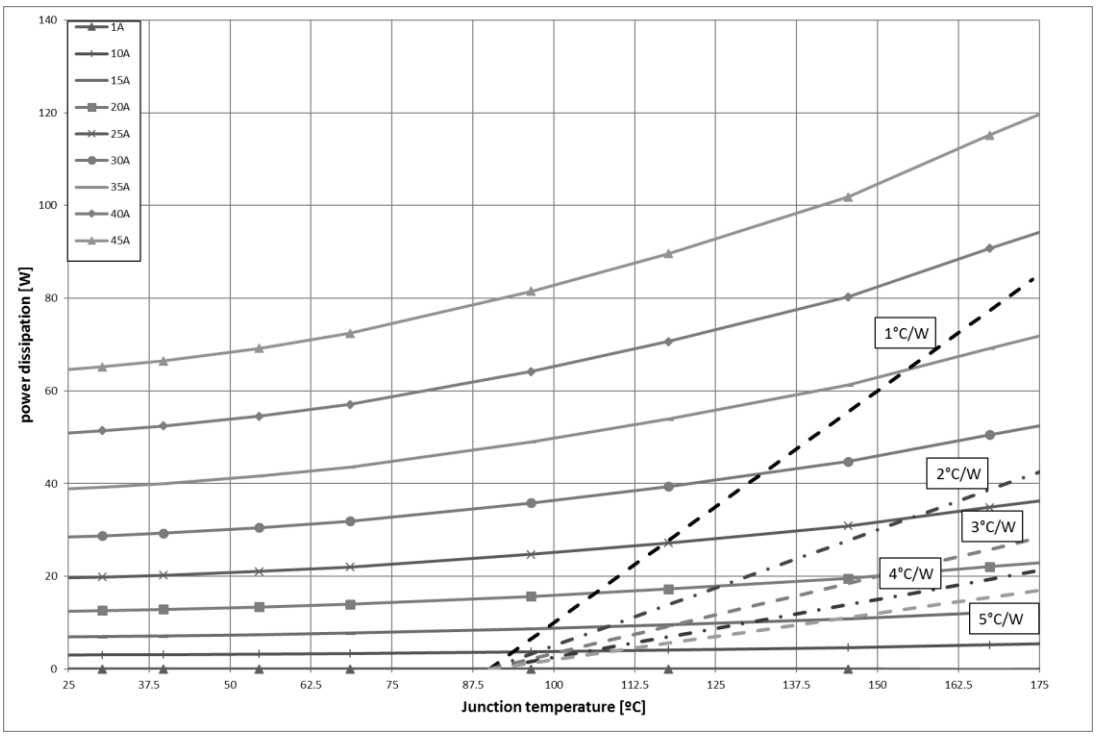
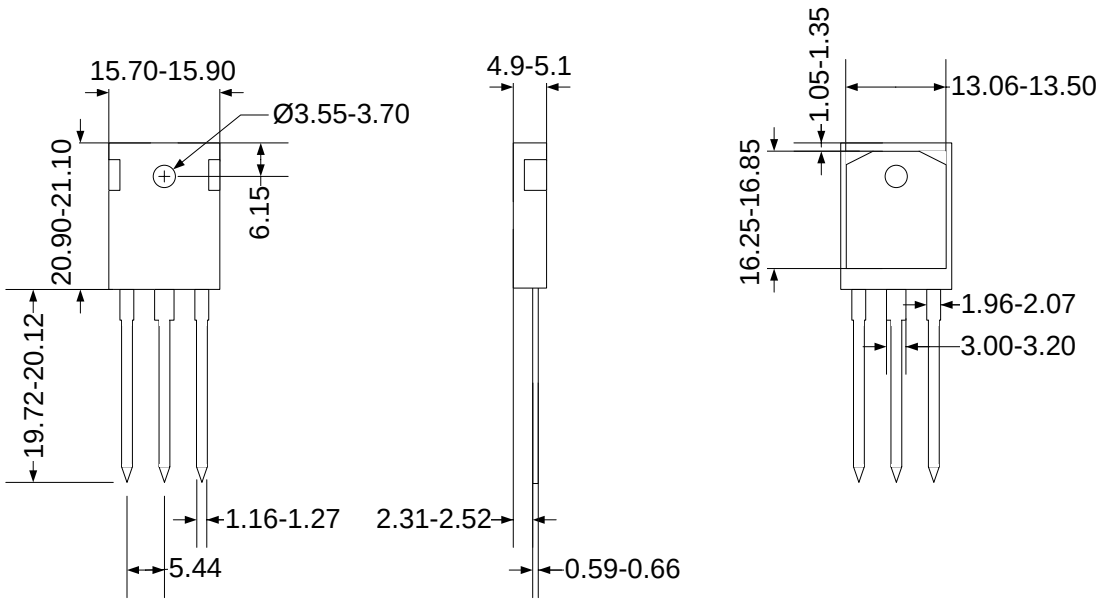


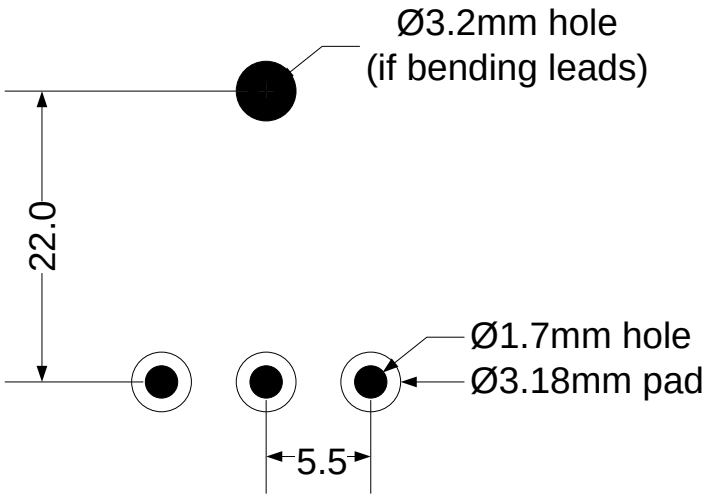
Figure 16: Thermal Safe Operating Area

Package Dimension

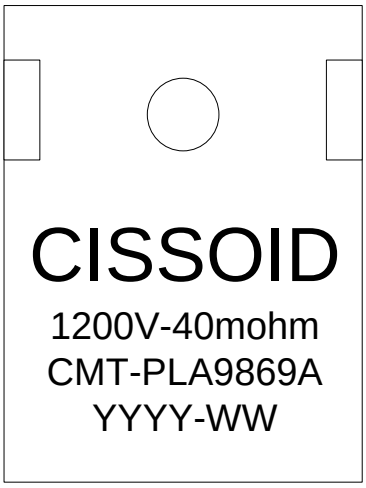


TO-247 physical dimensions (+/-0.2mm)

Suggested PCB Pad Layout



Marking information



YYYY	Year
WW	Week (1 to 53)

Ordering Information

Product Name	Ordering Reference	Package	Marking
CMT-PLA9869	CMT-PLA9869A-TO247	TO-247	CHT-PLA9869A

Contact & Ordering

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