CHT-VEGA-DATASHEET

Version: 2.5
20-Dec-23
(Last Modification Date)

High-Temperature, Low Dropout, Adjustable Voltage Regulator +1.2V to +3.3V / 500mA

General description

The CHT-VEGA is a high-temperature, high-reliability, 500mA adjustable linear voltage regulator suitable to generate from a standard +5V ±10% source any regulated voltage in the range +1.2V to +3.3V. Its typical operation junction temperature ranges from -55°C to +225°C and can possibly go outside that range with some de-rating of the performance. The regulator is self-protected with a built-in over-current limitation and a thermal protection, the later becoming effective in the range 250°C to 300°C. CHT-VEGA brings unique benefits in applications where the ambient or operating temperature is high and above the temperature supported by traditional semiconductors, or in applications that run in standard 125°C or 150°C, possibly 175°C but that require extended reliability: CHT-VEGA brings at least an order of magnitude in lifetime compared to traditional silicon solutions. It allows as well accelerated aging of the systems for qualification purposes as the device can support extreme temperatures.

The circuit is stable throughout the whole temperature range and only requires an external output capacitor and a 2-resistor bridge for feedback. The IC features a chip-enable (CE active low) input signal allowing placing the circuit in low-power, disable mode. The output voltage is adjustable by the external resistive feedback.

The CHT-VEGA is a one-die solution, available in a tiny ceramic package TDFP-16 for applications where small PCB footprint is critical. The TDFP package is an SMD solution with leads, available by default in 16-pin.

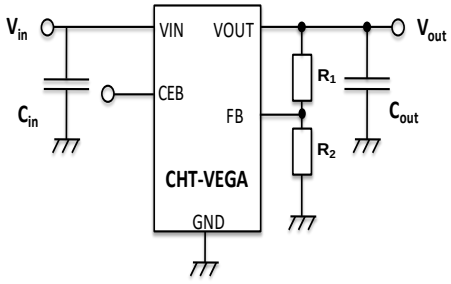
Features

- Junction operating temperature from -55°C to 225°C
- Input voltage from 4.5V to 5.5V
- Output voltage: from 1.2V to 3.3V
- Output voltage total accuracy: ±5%[1]
- Output current: 500mA max
- Line regulation: -0.2% typ
- Load regulation: -2%/A typ
- C_{out}: 1 to 10 µF ceramic low ESR
- Input ripple rejection: 67dB typ (@ 100Hz)
- Quiescent current (no load, Chip Enable active, 225°C): 1 mA typ.
- Stand-by current (no load, Chip Enable inactive, 225°C): 10 µA typ.
- Thermal shutdown: Active in the range 250°C to 300°C
- Current limitation: 1.15A (typ)
- Latch-up free
- Available in TDFP16 (other packages: contact CISSOID)
- Validated at 225°C for 5000 hours (and still on-going)

Applications

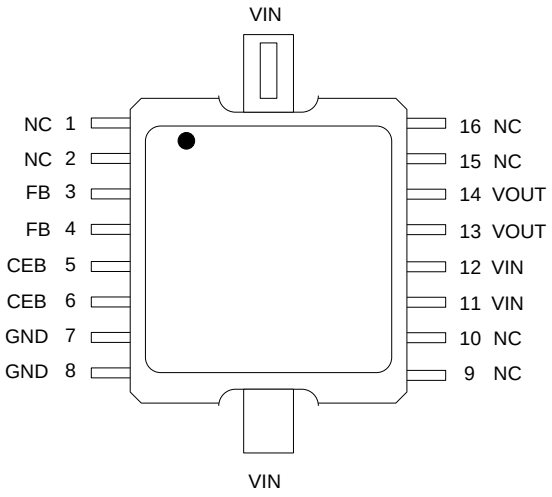
- Regulated power supply in down-hole, aerospace and industrial systems.

Typical Application



[1] Excluding accuracy of external components
but including initial accuracy variation, temperature variation, line and load regulation variations

Pinout



Pin #	Pin Name	Pin Description
1	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
2	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
3	FB	Input pin; feedback pin to be connected via a resistor network to Vout (cfr Typical application diagram on page 1)
4	FB	Input pin; feedback pin to be connected via a resistor network to Vout (cfr Typical application diagram on page 1)
5	CEB	Input pin; Chip Enable pin; when connected to GND, CHT-VEGA is active; when connected to VIN, VOUT is tied to GND and CHT-VEGA enters in a low-power mode
6	CEB	Input pin; Chip Enable pin; when connected to GND, CHT-VEGA is active; when connected to VIN, VOUT is tied to GND and CHT-VEGA enters in a low-power mode
7	GND	Negative power supply
8	GND	Negative power supply
9	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
10	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
11	VIN	Positive power supply
12	VIN	Positive power supply
13	VOUT	Output voltage
14	VOUT	Output voltage
15	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
16	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing

The 2 vertical large leads are internally connected to VIN and are also connected to the package heat sink. Those 2 vertical pins MUST be connected at PCB level to VIN

Absolute Maximum Ratings

Supply Voltage Vin to GND	-0.5 to 6V
Voltage on CEB and FB	max Vin
Peak output current	Internally limited
Junction Temperature (Tj)	250°C

ESD Rating

Human Body Model	Class1B

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability. Permanent uses of the device in short-circuit state or in over-temperature state may affect long term reliability of the device.*

Operating Conditions

Supply Voltage Vin to GND:	4.5V to 5.5V
Junction temperature	-55°C to +225°C
Continuous current	0 to 500 mA

Electrical Characteristics

Unless otherwise stated, T_j = 25°C, C_{in} = 1µF, C_{out}= 1µF . **Bold** figures point out values valid over the whole temperature range (T_j = -55°C to +225°C).

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Voltage	V_{in}		**4.5**	**5**	**5.5**	V
Output voltage range	V_{out}		**1.1**		**3.6**	V
Output current	I_{out}		**0**		**500**	mA
Output voltage total accuracy		Vin =[4.5-5.5]V Iout = [0 .. 500]mA	**Vout -5%**		**Vout +5%**	V
Output voltage temperature drift		Vin= 5V ; Vout = 1.8V Iout = 0mA T_j = [25°C -225°C]		+2.5		%
Output voltage line regulation		Vin =[4.5-5.5]V; Vout = 1.8V Iout= 0mA		-0.2		%
Output voltage load regulation		Vin =5V ; Vout = 1.8V Iout = [0 .. 500]mA		-1[1]		%
Quiescent current[2]	I_q	Vin= 5V ; Vout = 1.8V Iout = 0 mA	**0.8**	1	**1.4**	mA
Standby current3	I_{stdby}	Vin = 5V ; Vout = 1.8V Iout = 0 mA ; T_j = 25°C CEB = 5V			100	nA
		Vin = 5V ; Vout = 1.8V Iout = 0 mA ; T_j = 225°C CEB = 5V			20	µA
Response to Line Transient		Vin from 4.5V to 5.5V (1V/µs) Vout = 1.8V; Iout = 0mA		+2		%
		Vin from 5.5V to 4.5V (1V/µs) Vout = 1.8V;Iout = 0mA		-2		%
Response to Load Transient		Vin = 5V; Vout = 1.8V Iout from 0mA to 500 mA (10mA/µs)		-3		%
		Vin = 5V; Vout = 1.8V Iout from 500 mA to 0 mA (10mA/µs)		+3		%
Power Supply Rejection Ratio (Vin=5V, Vout=1.8V, Iout=0mA, ESR<0.2Ω)	PSRR	100Hz		67		dB
		1 KHz		55		dB
Average short-circuit current	Isc	Vin = 5V; Vout = 0V		1.15		A
Over current detection threshold	Ith	Vin = 5.5V; Vout = 1.2V		1.6		A
		Vin = 4.5V; Vout = 3.3V		0.88		A
FB input current	I_{FB}	V_{FB} = 0.9V +/- 10%		5		nA
CEB input current	I_{CEB}	Vin = 5V		10		nA
CEB V_{IL}	$V_{IL\ CEB}$	Vin = 5V			**2**	V
CEB V_{IH}	$V_{IH\ CEB}$	Vin = 5V	**3**			V
Over temperature protection threshold	TH_{OTP}			300		°C
Over temperature protection hysteresis	$Hyst_{OTP}$			30		°C
Junction–to-case thermal resistance	$R_{\Theta JC}$			11		°C/W

[1] Load regulation measurements must be done in a way to avoid self-heating effect

[2] Current through feedback resistances excluded

Typical Performance Characteristics

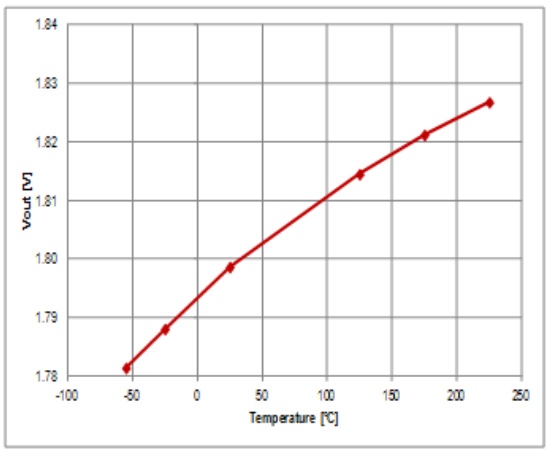


Figure 1: Output voltage temperature drift

(Vin =5V, Vout =1.8V, Iout = 0 mA)

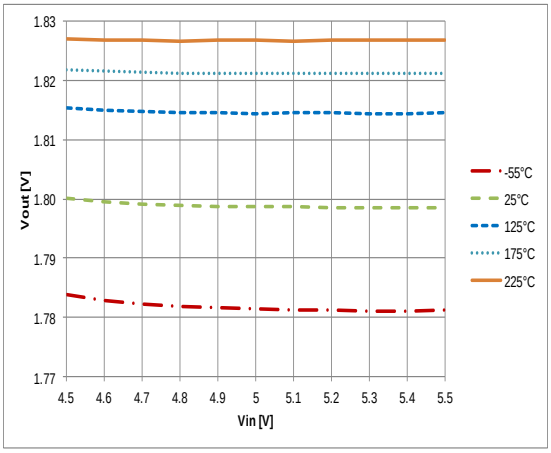


Figure 2: Output voltage line regulation (Iout = 0mA)

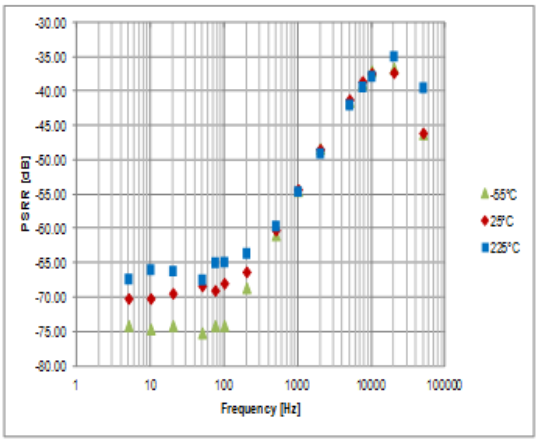


Figure 3: Input ripple rejection (PSRR)

(Iout=0mA, Vin=5V, Vout=1.8V, Cout = 1µF, ESR<0.2Ω)

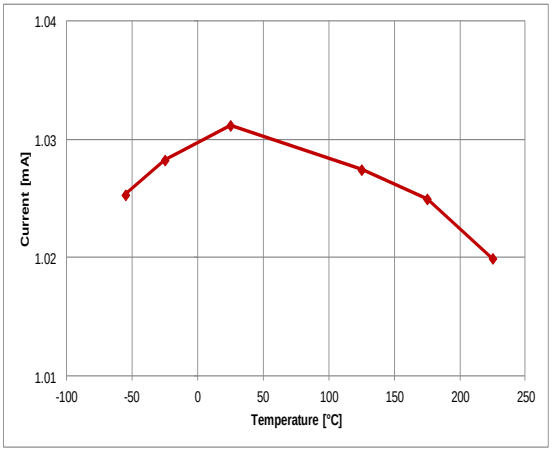


Figure 4: Iq versus temperature

(Vin = 5V, Vout = 1.8V, Iout = 0 mA)

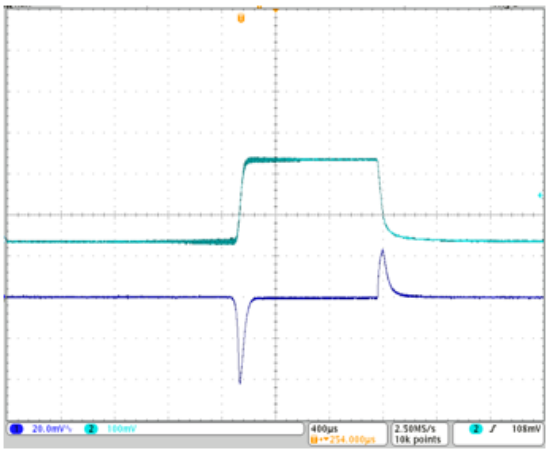


Figure 5: Response to load transient

(0A to 500 mA, 500 mA to 0A, Vin = 5V, Vout = 1.8V, Ta= 25°C) (1: Vout,2: Iout)

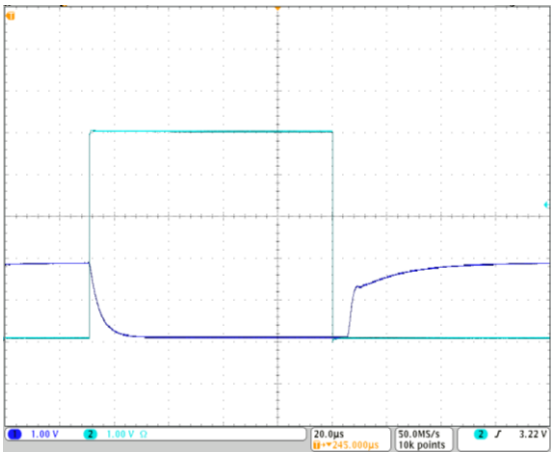


Figure 6: Transition to/from disabled state

(Vin =5V, Vout = 1.8V, Iout = 500 mA, Ta = 25°C) (1:Vout,2:CEB)

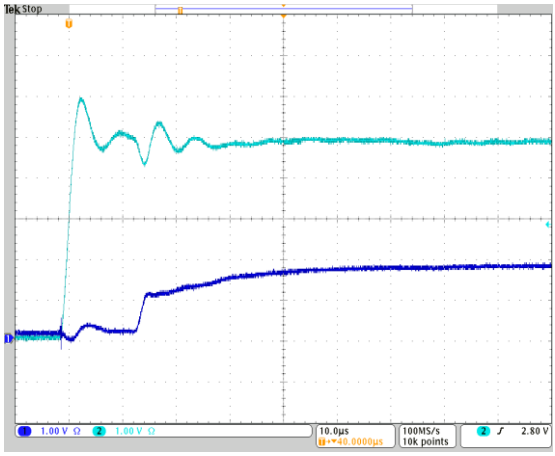


Figure 7: Start-up transient

(Vin = 0 to 5V; Vout = 1.8V, Iout = 500 mA, Ta = 25°C)

(1: Vout,2:Vin)

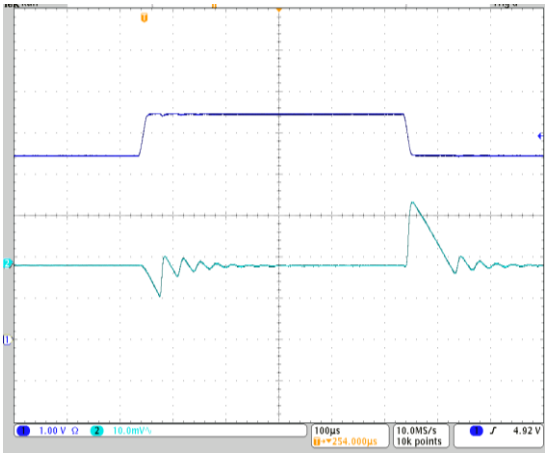


Figure 8: Response to line transient

(Iout = 0 mA, Vin: 4.5 to 5.5V, 5.5V to 4.5V, Vout = 1.8V, Ta= 25°C) (1:Vin,2:Vout AC)

Circuit Functionality

Safe operating area wrt to power dissipation including PCB layout guidelines

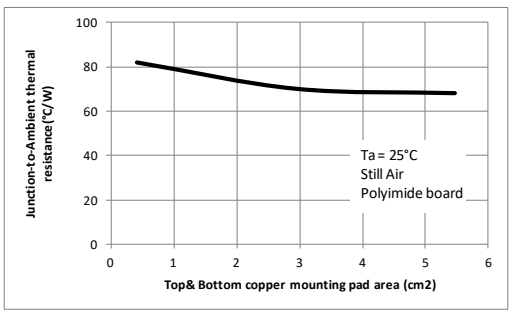
As the package used for CHT-VEGA is very small, achieving efficient thermal performance for power applications requires efficient management of the heat flow out of the device. The purpose of this section is to guide the user in maximizing the power handling capability of the TDFP16 package. Using natural cooling, the method of improving power performance should be focused on the optimum design of copper mounting pads. The design should take into consideration the size of the copper and its placement on either or both of the board surfaces. A copper mounting pad is important because the substrate of the integrated circuit is mounted directly onto the thermal pad of the TDFP16 package. The pad acts as a heat sink to reduce thermal resistance and leads to improved power performance.

The maximum power dissipation is determined by the maximum junction temperature rating, the ambient temperature, and junction-to-ambient thermal resistance:

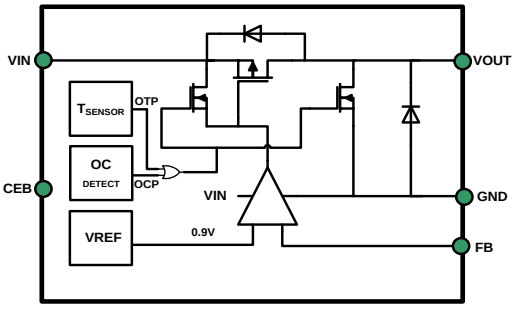
$$P_{DMAX} = (T_{JMAX} - T_A)/R_{\theta JA}$$

Where T_{JMAX}=225°C and $R_{\theta JA}=R_{\theta JC}+R_{\theta CA}$ with $R_{\theta JC}$=11°C/W and $R_{\theta CA}$ (to be determined) is function of the size of the copper mounting pad and thermal coupling to the TDFP16.

The graph below provides information about junction-to-air thermal resistance of the package mounted on PCB with different sizes of copper thermal pads.

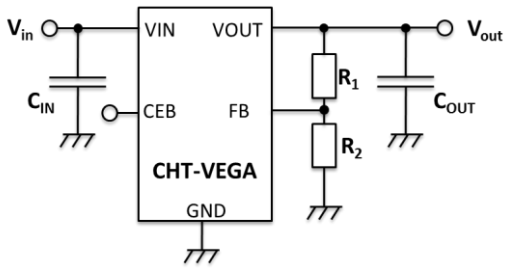


Functional Block diagram



A PMOS transistor controls the level of current flowing from VIN to VOUT. An internal voltage reference of 0.9V (highly stable over the whole temperature range) provides the reference to which the voltage on the FB pin is compared. The internal amplifier drives the gate of the PMOS and regulates VOUT.
An on-chip temperature sensor with hysteresis measures the die temperature; if this temperature exceeds a predefined threshold, the PMOS transistor is disabled and VOUT is connected to GND.
An overcurrent protection circuit is implemented. When the output current is reaching a certain threshold (Ith), the PMOS transistor is disabled and VOUT is connected to GND for a certain period of time (typ 0.5 µsec); then normal operation is resumed. So in case of eg permanent short-circuit, the overcurrent protection mechanism will alternate between 2 states (ON, OFF) and deliver an average current of 1.15A (typ).
CEB pin provides a Disable feature (when CEB is high, CHT-VEGA is disabled); internally, this signal acts in the same way as the over temperature detection signal (OTP).

External resistances calculation rules



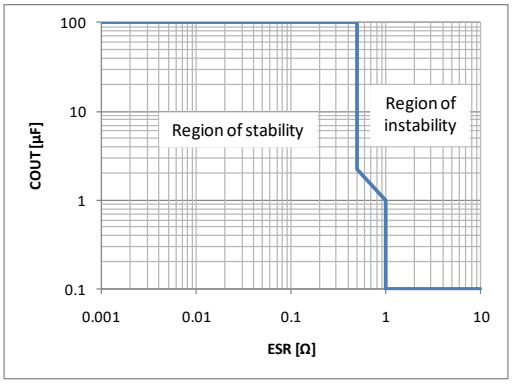
R1 and R2 values should be computed as follows:

$$\frac{R1+R2}{R2}=\frac{VOUT}{0.9V}$$

R1+R2 value should be lower than 200kΩ to limit the impact of the FB input leakage current.

ESR/Cload graph

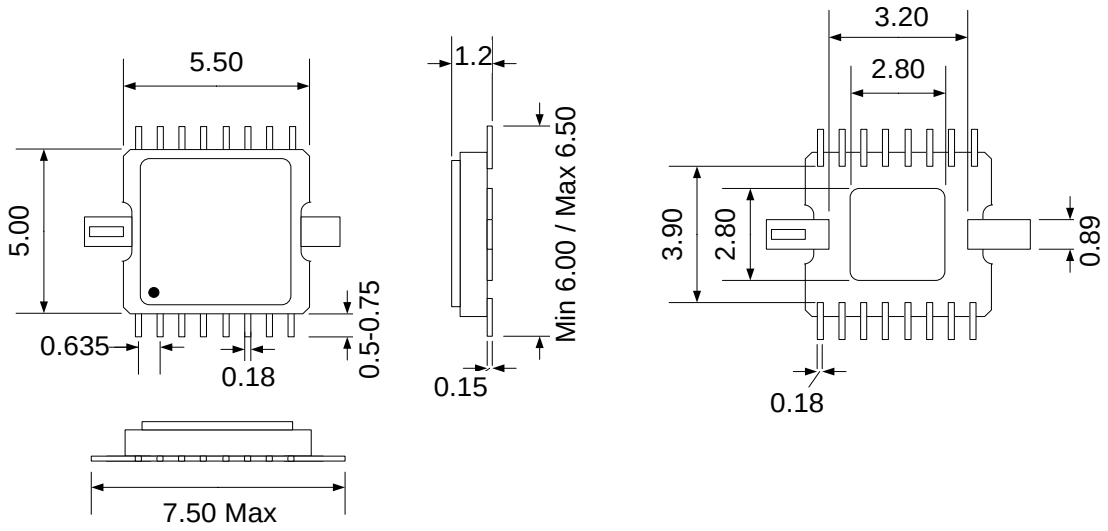
The output capacitor of the regulator must be selected in the region of stability indicated by the figure below.
Even though still in the stability region, capacitances less than 1 µF should be used with care because they require careful selection of ESR to ensure stability.



Input capacitance

Recommended typical value for the C_{IN} capacitance is 1µF.

Package Dimensions



TDFP16 physical dimensions (mm +/- 10%)

Ordering Information

Product Name	Ordering Reference	Package	Marking
CHT-VEGA	CHT-STA4853B-TDFP16-T	TDFP16	CHT-STA4853B

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 11 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: sales@cissoid.com
Sales Representatives:	**Visit our website: http://www.cissoid.com**

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