CHT-MAGMA DATASHEET

Version: 1.15
20-Dec-23
(Last Modification Date)

High Temperature PWM Controller

General Description

MAGMA is a High Temperature Pulse Width Modulation (PWM) Controller with maximum duty cycle up to 90%. It operates at constant frequency, adjustable from 50KHz up to 500KHz.

MAGMA can operate with input voltages from 6 to 30V. It also features an internal voltage reference, input feed forward compensation making it less sensitive to input voltage variations, and a soft start activated whenever MAGMA comes out of stand-by or the output is enabled.

An under-voltage lockout function maintains the PWM output low until the controller has sufficient supply voltage for proper operation. A “power good” comparator returns a “good” signal when the DC-DC converter output voltage has reached a programmable threshold. A synchronization pin can be driven by an external clock while the internal clock is available on *CKOUT* pin.

Features

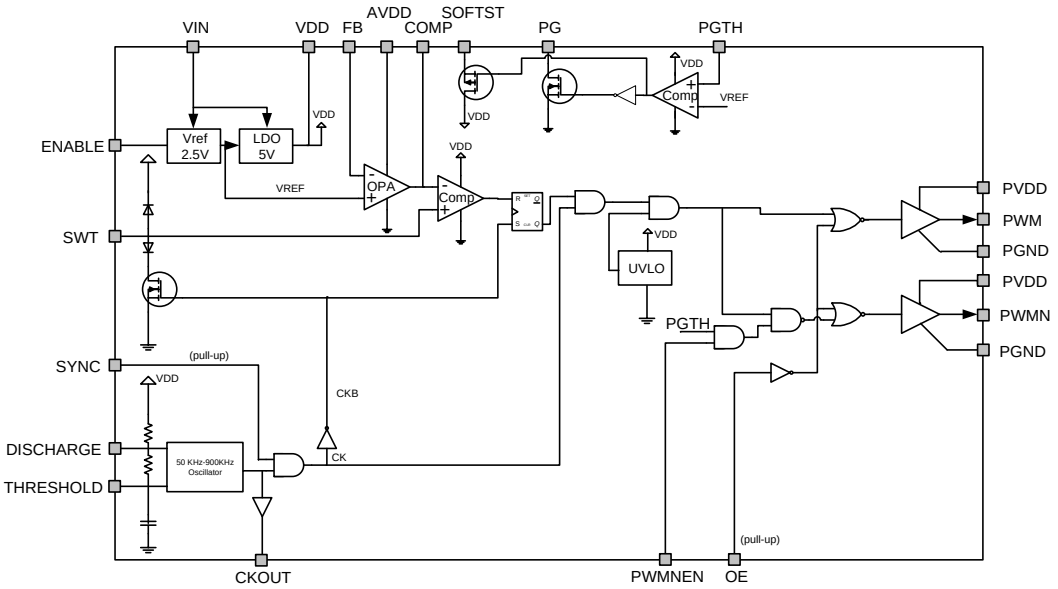
- Voltage Mode PWM Controller
- Adjustable Max Duty Cycle up to 90%
- Constant Switching Frequency adjustable between 50KHz to 500KHz
- Input Voltage from 6V to 30V
- Input Voltage Feed Forward Compensation
- On-chip 2.5V Reference Voltage
- Stand-by Mode
- Under Voltage Lockout
- Soft-Start Capability
- Synchronization Capability
- Power Good Flag
- Output Enable
- Validated at 225°C for 43700 hours (CDIL28)/20000 hours(CSOIC28) (and still on-going)

Applications

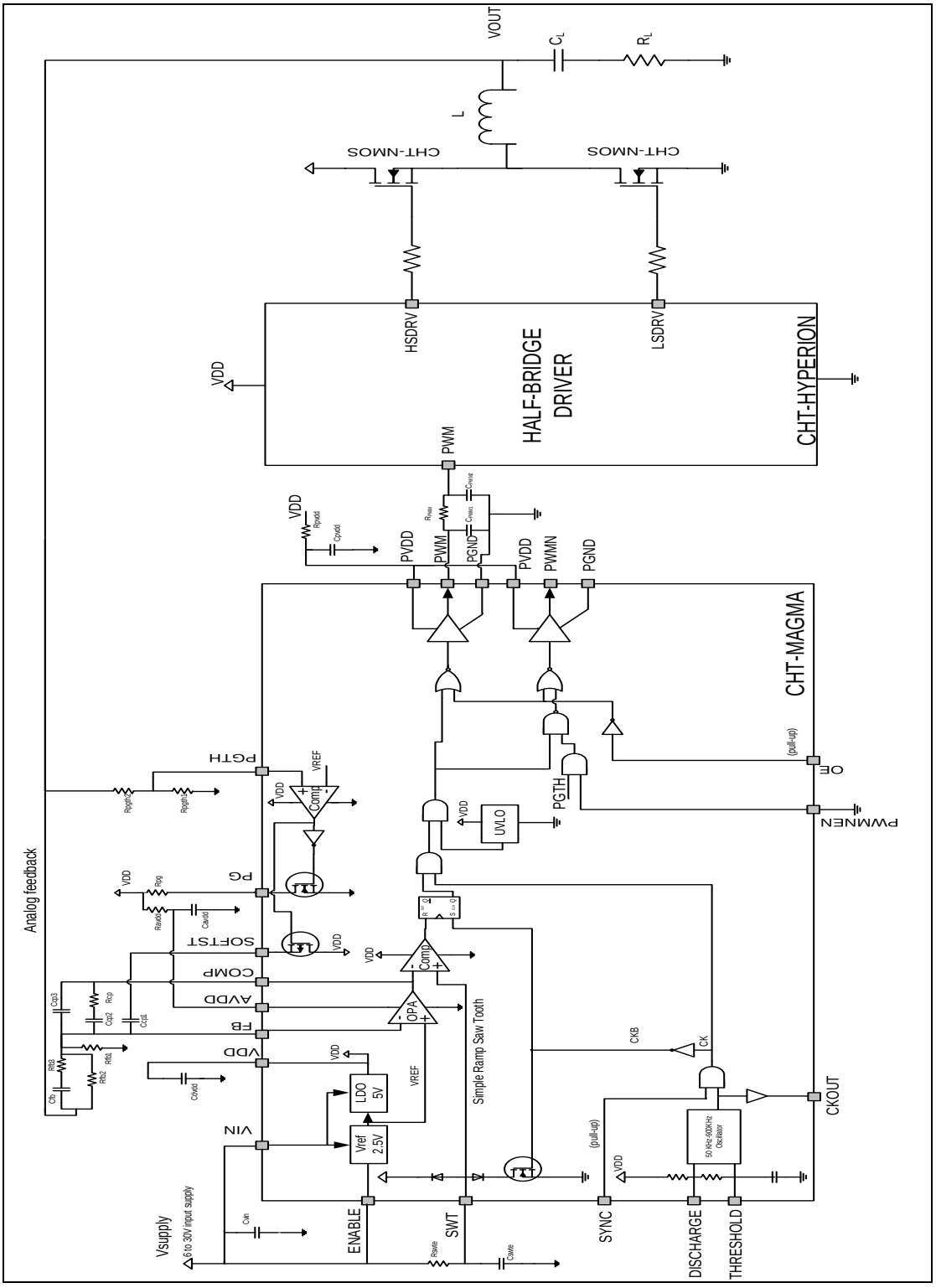
DC-DC Converters in Oil&Gas, Industrial, Aerospace & Automotive.

Refer to http://www.cissoid.com/files/files/products/volcano/cht-magma.pdf for latest datasheet version.

Functional Block Diagram



Typical Application: 5V DCDC BUCK CONVERTER



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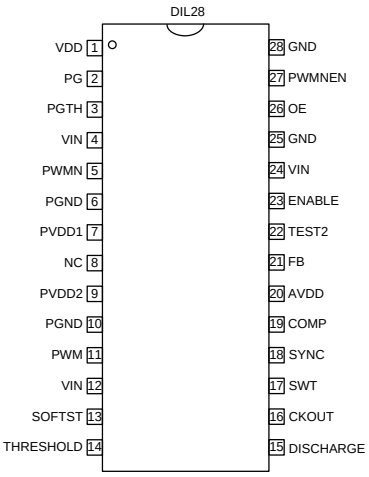
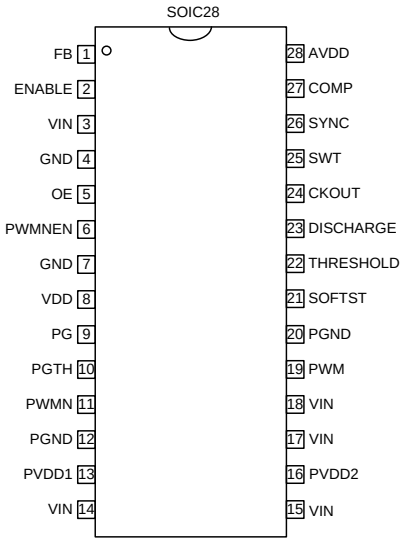
[1] Typical values for R_{pwm} and C_{pwm2} are : R_{pwm} = 220Ω and C_{pwm2}= 47 pF ; max value for C_{pwm2} : 100 pF Same recommandations/requirements apply to PWMN pin.

Package Configurations: CDIL28



Pin #	Pin Name	Pin Description
1	VDD	5V **output** of the internal LDO. This node needs to be externally decoupled and connected to other VDD, AVDD and PVDD.
2	PG	“Power Good”. When the voltage on “PGTH” is lower than 2.5V, PG is pulled down. Otherwise, PG presents a high impedance. If used, this pin requires an external pull-up resistor.
3	PGTH	“Power Good Threshold”. This node is compared to the internal 2.5V reference. If PGTH<2.5V, PG is pulled down and SOFTST is pulled up. If PGTH>2.5V, PG and SOFTST present a high impedance.
4	VIN	Input supply of the LDO.
5	PWMN	Inverse (non-overlapped wrt to PWM on the falling PWMN edge) of “pulse Width Modulation” signal (5V logic level) (cfr General Description Section for more information)
6	PGND	Power ground of the PWM output buffer. Connect to ground.
7	PVDD1	Power supply of the PWM output buffer. Connect to VDD (pin1) with a 10Ω resistor and decoupling capacitance.
8	NC	Not connected
9	PVDD2	Connect to pin7
10	PGND	Power ground of the PWM output buffer. Connect to ground.
11	PWM	“Pulse Width Modulation” output (5V logic level).
12	VIN	Input pin. To be connected at PCB level with other VIN pins.
13	SOFTST	“Soft Start”. An external capacitor must be connected between this node and the “FB” node. As long as the voltage on PGTH node is lower than 2.5V, SOFTST is internally pulled up to VDD.
14	THRESHOLD	Node of the internal oscillator. Reduce as much as possible parasitic capacitances on this node if the internal oscillator is used.
15	DISCHARGE	Node of the internal oscillator. Left this pin floating for the default 230kHz frequency.
16	CKOUT	The waveform on this node is a copy of the internal oscillator. It can be used for synchronisation purposes between various PWM controllers.
17	SWT	When the internal clock is low, SW is pulled down to approximately a forward diode voltage. An external RC must be connected on this node in order to generate a saw-tooth. Connecting the resistor to the input supply allows having a saw tooth slope proportional to the supply (input feed-forward).
18	SYNC	An external 5V clock can be applied on this node for synchronization purposes. In this case, the internal clock must be deactivated (connecting the “DISCHARGE” to ground). Note that the output PWM duty cycle cannot be larger than the duty-cycle of the external clock. If not used, SYNC must be floating or connected to VDD.
19	COMP	Output of the internal error amplifier & input of the PWM comparator.
20	AVDD	Analog 5V supply of the error amplifier. Connect to a well decoupled 5V source.
21	FB	Negative input of the error amplifier.
22	TEST2	Internal test node. Left floating
23	ENABLE	If grounded, the internal LDO is turned off and the PWM output is set to zero. A voltage between 4V and VIN on this node activates the LDO and allows a normal operation of the PWM output.
24	VIN	Input supply of the LDO.
25	GND	Ground pin
26	OE	Output Enable. Internally pulled-up to VDD. If low, it sets the PWM output to zero.
27	PWMNEN	Enable of PWMN signal (active high)(cfr General Description Section for more information)
28	GND	Ground pin

Package Configurations: CSOIC28



Pin #	Pin Name	Pin Description
1	FB	Negative input of the error amplifier.
2	ENABLE	If grounded, the internal LDO is turned off and the PWM output is set to zero. A voltage between 4V and VIN on this node activates the LDO and allows a normal operation of the PWM output.
3	VIN	Input supply of the LDO
4	GND	Ground pin
5	OE	Output Enable. Internally pulled-up to VDD. If low, it sets the PWM output to zero.
6	PWMNEN	Enable of PWMN signal (active high)(cfr General Description Section for more information)
7	GND	Ground pin
8	VDD	5V **output** of the internal LDO. This node needs to be externally decoupled and connected to other VDD, AVDD and PVDD.
9	PG	“Power Good”. When the voltage on “PGTH” is lower than 2.5V, PG is pulled down. Otherwise, PG presents a high impedance. If used, this pin requires an external pull-up resistor.
10	PGTH	“Power Good Threshold”. This node is compared to the internal 2.5V reference. If PGTH<2.5V, PG is pulled down and SOFTST is pulled up. If PGTH>2.5V, PG and SOFTST present a high impedance.
11	PWMN	Inverse (non-overlapped wrt to PWM on the falling PWMN edge) of “pulse Width Modulation” signal (5V logic level) (cfr General Description Section for more information)
12	PGND	Power ground of the PWM output buffer. Connect to ground.
13	PVDD1	Power supply of the PWM output buffer. Connect to VDD (pin8) with a 10Ω resistor and decoupling capacitance.
14	VIN	Input supply of the LDO
15	VIN	Input supply of the LDO
16	PVDD2	Connect to pin13
17	VIN	Input supply of the LDO
18	VIN	Input supply of the LDO
19	PWM	“Pulse Width Modulation” output (5V logic level).
20	PGND	Power ground of the PWM output buffer. Connect to ground.
21	SOFTST	“Soft Start”. An external capacitor must be connected between this node and the “FB” node. As long as the voltage on PGTH node is lower than 2.5V, SOFTST is internally pulled up to VDD.
22	THRESHOLD	Node of the internal oscillator. Reduce as much as possible parasitic capacitances on this node if the internal oscillator is used.
23	DISCHARGE	Node of the internal oscillator. Left this pin floating for the default 230kHz frequency.
24	CKOUT	The waveform on this node is a copy of the internal oscillator. It can be used for synchronisation purposes between various PWM controllers.
25	SWT	When the internal clock is low, SW is pulled down to approximately a forward diode voltage. An external RC must be connected on this node in order to generate a saw-tooth. Connecting the resistor to the input supply allows having a saw tooth slope proportional to the supply (input feed-forward).
26	SYNC	An external 5V clock can be applied on this node for synchronization purposes. In this case, the internal clock must be deactivated (connecting the “DISCHARGE” to ground). Note that the output PWM duty cycle cannot be larger than the duty-cycle of the external clock. If not used, SYNC must be floating or connected to VDD.
27	COMP	Output of the internal error amplifier & input of the PWM comparator.
28	AVDD	Analog 5V supply of the error amplifier. Connect to a well decoupled 5V source.

Absolute Maximum Ratings

Devices stressed above these absolute maximum ratings could present permanent damage. Exposure to this maximum rating for extended periods may affect the device reliability. These ratings are considered individually (not in combination). If not specified, voltages are related to the ground GND.

Parameter	Min.	Max.	Units
VIN	-0.3	40	V
VDD	-0.3	7	V
OE, SYNC, PWMNEN	-0.3	“VDD”+0.3	V
PWM, PWMN	-0.3	6	V
PGND	-0.3	0.3	V
PVDD1, PVDD2, AVDD	“VDD”-0.3	“VDD”+0.3	V
Junction Temperature		250	°C
ESD Rating (Human Body Model)	1 (expected)		kV

With high voltage/high frequency switching, parasitic inductors and capacitors could create current and voltage glitches beyond the absolute maximum rating. So, it is recommended to take special care when developing your application to minimize parasitic at PCB level on all high voltage nodes to prevent exceeding absolute maximum rating.
Also, probing on PWM and PWMN pins should be done with a lot of care; it is recommended to not perform any hot probing on those nodes.

Electrical Characteristics

Unless otherwise stated: V_{DD}=5V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Input Supply					
VIN supply		**6**		**30**	V
I(VIN)[1]	internal oscillator at 230kHz Vin=7V, 25°C		1.3		mA
Digital Input Controls (OE; SYNC, PWMNEN)					
Input Current	Internal pull-up	**25**		**85**	µA
High level input voltage		**3.7**		**VDD+0.3**	V
Low level input voltage		**-0.3**		**2**	V
Analog inputs[2]					
PGTH, FB, THRESHOLD, DISCHARGE		**0**		**VDD**	V
ENABLE	Low level[3] High level	 **3**		**0.5** **VIN**	V V
Input current	(Mostly from ESD diode)	**-100**		**100**	nA
Digital outputs					
PWM	Low level @100mA High level @100mA	 **VDD-0.5**		**0.5**	V V
PG[4]	Pull down only. R_{ON} value	**1k**		**4k**	Ω
CKOUT	Low level @2mA High level @2mA	 **VDD-0.5**		**0.5**	V V
PWMN	Low level @100mA High level @100mA	 **VDD-0.5**		**0.5**	V V
t_{NOVR}: Non-overlap delay between falling PWMN edge and rising PWM edge			60		ns
t_{DEL}: Delay between rising PWMNEN edge and rising PWMN edge	Assuming PWMN internal signal is HIGH before PWMNEN rising edge		20		ns
Under Voltage LockOut (UVLO)					
VDD threshold for PWM enabling[5]	-55°C 25°C 125°C 225°C		4.2 3.8 3.3 2.8		V V V V

[1] See Figure 2.
[2] Above 5V or bellow 0V, the ESD diode becomes forward biased.
[3] When low, the internal LDO is turned OFF. VDD should therefore go to zero. However, due to the input feedforward resistor used on the node SWT, VDD could rise slightly above zero.
[4] PG is ESD protected versus GND and VDD. The pull-up resistor should be connected to a voltage smaller or equal to VDD.
[5] Above this threshold, the PWM modulator is functional. Bellow this threshold, the PWM output is low.

Electrical Characteristics (continued)

Unless otherwise stated: V_{DD}=5V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
OPA					
Output voltage swing		**0.15**		**AVDD-0.2**	V
Output current			**±15**		mA
Input offset voltage			±2.5	±8	mV
Input offset drift			±5	±15	µV/°C
DC gain	Tj=25°C Tj=225°C		100 87		dB dB
Gain-bandwidth product	Cload=30pF, RL=2kΩ	**1.3**	**1.5**		MHz
Power supply rejection ratio	0-100Hz	**78**			dB
Slew rate	Cload=30pF, RL=2kΩ Tj=25°C Tj=225°C	 1.0 1.6	 1.2 1.7		 V/µs V/µs
Phase margin	Cload=30pF, RL=2kΩ	**50**	**>60**		Degree
Integrated input noise	DC to 10Hz		**25**		μV_{RMS}
Input current (“FB” pin)				**±10**	nA

Voltage Reference (2.5V)					
Accuracy	Tj=125°C; Vin=7V	2.45 -2	2.5	2.55 +2	V %
Temperature drift	See Figure 4	**+100** **+25**	**+250** **+100**	**+400** **+160**	µV/°C ppm/°C
Line regulation	See Figure 4	**-1.5**		**+1.5**	mV/V
Minimum dropout (Vin-Vref)[1]			**0.7**		V

5V linear regulator (LDO)					
VDD accuracy	Tj=125°C; Vin=7V	4.6 -8	5	5.4 +8	V %
Load current[2]		**0**		**25**	mA
Temperature drift	Vin=7V	**-1**		**+2**	mV/°C
Load Regulation	Vin=7V Tj=25°C Tj=225°C	 1.2 2.7		 2.3 3.6	 mV/mA mV/mA
Line Regulation	Tj=25°C Tj>125°C	-2 -1		+10 +6	mV/V
Min. dropout (Vin-VDD)[3]	I_{load}=0mA		**0.5**		V
Input capacitance required	Ceramic or other low ESR	**470**			nF
Output capacitance required[4]	Ceramic or other low ESR	**220**		**2200**	nF

PWM modulator (comparator, RS flip-flop, logic, output buffer)					
Input range (COMP, SWT)[5]		**-0.3**		**VDD+0.3**	V
Delay to PWM (goes up)[6]	PWM goes up		**100**		ns
Delay to PWM (goes down)[7]	FAST slope Slope=5V/µs Slope=1V/µs		**220** **320** **720**		ns ns ns
Duty Cycle		**0**		**D(ck)**[8]	%

[1] The **dropout** is defined as the input voltage minus the output voltage (Vref). The **“minimum dropout”** is defined as the dropout for which the local line regulation (δVref/δVin) is better than 10mV/V and Vref>2.4V.
[2] The LDO is internally supplying most parts of the PWM controller. The load current considered here is an extra current (in order to supply an external driver for example).
[3] The **dropout** is defined as the input voltage minus the output voltage (VDD). The **“minimum dropout”** is defined as the dropout from which the local line regulation (δVDD/δVin) is better than 20mV/V and VDD>4.3V.
[4] Additional load capacitance can be used if they have an ESR of at least 10Ω.
[5] The comparator inputs are the pins COMP & SWT. As COMP is also the output of the buffered OPA (error amplifier), no external input signal can directly be applied on COMP node.
[6] Delay measured vs. the rising edge of the SYNC input (with the internal oscillator turned off)
[7] Delay measured versus the crossing of a positive edge on the SWT node and Vref (with SYNC high and COMP sets to Vref using the OPA as a follower). Different SWT raising slopes are considered. At first order, the worst case delay as function of the SWT slope (expressed in V/µs) can be approximated as 220ns+500ns/(SWT_slope[V/µs]) .
[8] The maximum PWM duty cycle cannot exceed the clock (SYNC or internal oscillator) duty cycle.

Electrical Characteristics (continued)

Unless otherwise stated: V_{DD}=5V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Internal oscillator (natural frequency)					
frequency[1]	THRESHOLD and DISCHARGE pads disconnected		230		kHz
Duty cycle	THRESHOLD and DISCHARGE pads disconnected	**89**	**91**	**93**	%
Frequency drift with temperature	THRESHOLD and DISCHARGE pads disconnected		0.18		kHz/°C
Internal oscillator (adjusting frequency) (See details in section "Clock signal" (page 11)					
Adjustable frequency range		20	230	700	kHz
Adjustable duty cycle		60		95	%
"Power Good" control					
Threshold	versus the internal Vref (2.5V)	-20	0	20	mV
Delay "PGTH" to "PG"[2]			100		ns
Saw tooth (SWT)[3]					
Discharge current[4]	Occurs when the oscillator (ck) is low. • V(SWT=5V) • V(SWT=2V)	 **20** **10**		 **60** **20**	 mA mA
Floating impedance[5]	Occurs when the oscillator (ck) is high.		500		kΩ
Minimum SWT voltage	SWT voltage for which the discharge current is smaller than 100µA (for ck low) • Tj=-55°C • Tj=200°C		 0.9 0.55		 V V

[1] As the internal oscillator capacitance is only 130pF, any additional parasitic capacitors on pins "THRESHOLD" and "DISCHARGE" can decrease the oscillation frequency.
[2] This delay is defined as the time between a voltage step (5V; 5ns slope) on PGTH and the switching of the PG pull down transistor. The output slope of PG then mostly depends on the external RC elements on this node. The delay is symmetrical versus the PGTH slope.
[3] The SWT pin is an analog input with ESD diode protection to gnd and VDD. Above 5V or bellow 0V, the ESD diode becomes forward biased.
[4] See Figure 1
[5] When the SWT discharge transistor is OFF, the SWT node internally sees a 500kΩ resistor connected to an internal 2.5V voltage source.

Typical Performance Characteristics

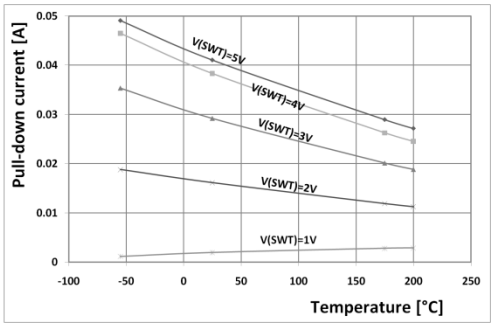


Figure 1: "SWT" pin pull-down current (when clock is low) over temperature as function of the SWT voltage.

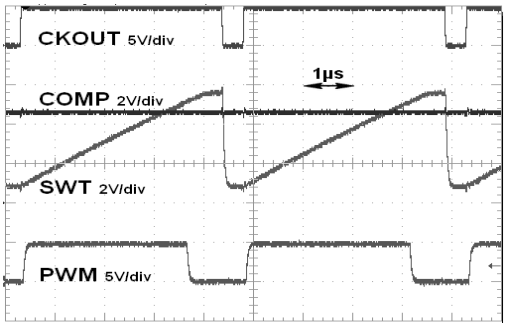


Figure 3: Typical waveform measured at 25°C on CKOUT, COMP, SWT and PWM nodes.

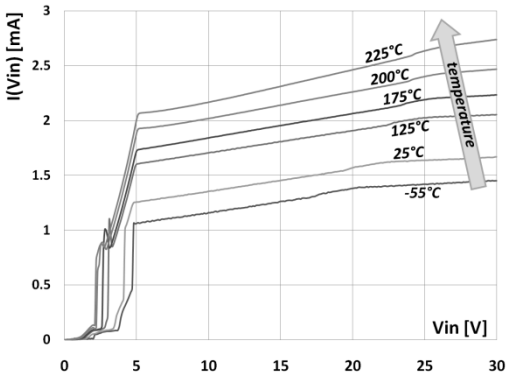


Figure 2: Total current consumption over temperature vs. input supply[1]

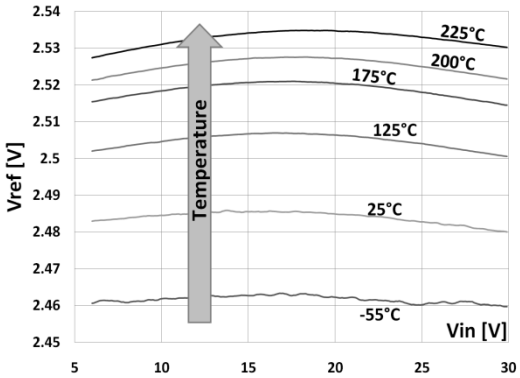


Figure 4: Typical internal voltage reference dependence on V_{in} and temperature.

[1] Measurement conditions: Use of the internal 230kHz oscillator; 100kΩ on the PG pad; 47kΩ between Vin and SWT; FB and PGTH to gnd; 30pF on the PWM output. If the internal oscillator is turned off, the current consumption is lowered by about 320µA (not represented in this figure).

General Description

The CHT-MAGMA circuit integrates a versatile pulse-width-modulation controller. The different blocks shown in the Functional Block Diagram section (page 2) are described hereafter. For these explanations, it is considered that the CHT-MAGMA is used in its typical application (5V DCDC buck converter) as sketched in page 2.

Error amplifier

It compares a fraction of the dc-dc converter output to the internal 2.5V reference. Its output V_{comp} is further compared to a saw-tooth in order to create a PWM signal.

Clock signal

The PWM controller is synchronized by a clock signal. This clock can either be internal or external (from SYNC node). In this last case, the internal clock needs to be turned off (connecting DISCHARGE to ground). The recommended frequency range is between 50kHz and 500kHz. Also, the duty-cycle of ck fixes the maximum duty-cycle of the PWM output. The positive edge of ck induces the positive edge of the PWM output after some delay (see delay in the Electrical Characteristics section). By default (when DISCHARGE and THRESHOLD are floating), the internal oscillator generates a typical ck signal of 230kHz at 25°C with a 90% duty cycle; this is based on following values for internal passive components:

- R between Vdd and DISCHARGE: 38.8KΩ
- R between DISCHARGE and THRESHOLD: 4.85KΩ
- C between THRESHOLD and GND: 130 pF.

External passive components can be used to change the default oscillator frequency; the clock frequency is then defined the following formula:

- Fclk= 1.44/[(Ra + 2 Rb)*C]
- DC (%) = 100*(Ra+Rb)/Ra+2*Rb where
- Ra is between Vdd and DISCHARGE
- Rb is between DISCHARGE and THRESHOLD

C is between THRESHOLD and GND.

Saw-tooth & input feed-forward.

The saw-tooth is generated by external Rswte and Cswte elements on the “SWT” pad (see the Typical Application 5V DCDC BUCK CONVERTER figure on page 2). The beginning of the charge of a series RC circuit is quite linear as long as the charge time is smaller than the RC constant. Each time ck goes low, the Cswte capacitor is quickly discharged by the SWT pad and remains discharged as long as the ck signal is low. In practice, the minimum discharge voltage is about a forward diode voltage (~0.7V at 25°C).

PWM modulator

Figure 3 depicts a typical measurement on node SWT, COMP, CKOUT and PWM.

PWM output

Due to the high driver strength on PWM output pin, it is mandatory to connect PWM pin to a serial resistor (Rpwm) in order to damp glitches during switching phase. Cissoid recommends a resistance value of 220 Ω. Maximum external capacitance on this node is 100 pF

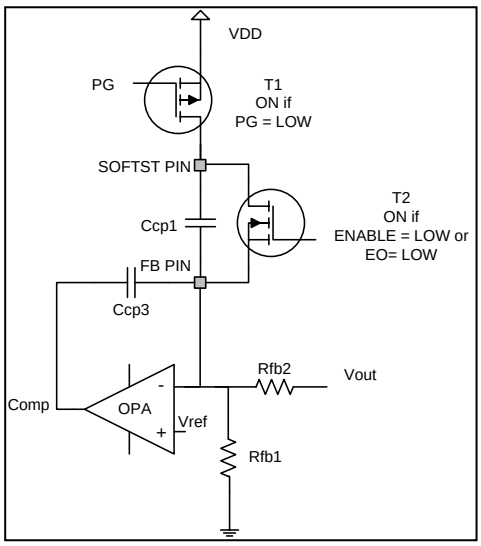
Power Good

The Power Good block (top right of the Functional Block Diagram figure) provides two different functionalities. By sensing a fraction of an output voltage (on PGTH pin) and comparing it to the internal 2.5V voltage reference, this block allows to activate the “PG” output flag and to deactivate the soft-start regime (see next section). Typically, for a 5V DCDC buck converter for example, the threshold of the power good is set to about 90% of the steady state DC output voltage, i.e. 4.5V. Resistors R_{pgth2} and R_{pgth1} of the Typical Application 5V DCDC BUCK CONVERTER figure should therefore be set in such a way that when the output voltage is 4.5V, the PGTH voltage is 2.5V.

Soft-start

When the input supply is connected and when the circuit is enabled, the output voltage should smoothly go from zero to its nominal voltage without overshoot (or smaller than about 10%) in order to protect sensitive loads.
Internally, the soft-start is also responsible for limiting the “inrush” current in a DCDC converter inductor. Such large current can

produce large glitches that could damage the power driver.
Unlike other implementations acting on VREF, CHT-MAGMA acts on FB node to implement the Softstart function.
The implementation needs to ensure that at start-up (or at restart), FB node is first pulled well above VREF to ensure %0 duty-cycle PWM and then needs to control the Vout rising speed. Softsart function in MAGMA works as follows:



- When MAGMA device is in disable state (either signal ENABLE or OE low), Ccp1 is internally shorted by a transistor (T2). SOFTST node is connected to VDD via an internal switch (T1) controlled by PG node (switch ON when PG=0). Consequently, with PG=0, SOFTST node voltage will be close to VDD, while FB voltage will be determined by the resistive divider made of the internal switches impedance (T1+T2) and the external feedback loop impedance; the external loop filter DC impedance (Rfb1 // Rbf2) should have a value higher than 34KΩ to make sure that FB voltage is well above 2.5V in all conditions (temperature, power supply, process variation). With FB voltage being above VREF, COMP node is at its lowest level, leading to the situation where the PWM controller is in a “minimum duty cycle” situation (0% duty cycle)
- When the switch (T2) over Ccp1 is turned off (both EN and OE are “high”), FB node voltage will decrease with a time constant defined by Ccp1 and by the feedback network DC impedance (the impedance of PG controlled switch T1 is negligible in this situation). During this period, the DC/DC feedback loop is still not active, ie COMP and VOUT are still at “0”
- When FB voltage crossed VREF, the DC/DC feedback loop starts to operate and FB node will be maintained at 2.5V by the feedback loop; however, the loop is still controlled by Ccp1 capacitance; indeed, Ccp1 is still being charged (SOFTST node will rise till VDD) through PG controlled switch (T1); this is the effective soft start period since the Ccp1 charge current is controlling the rise of Vout; the time constant is defined by Ccp1 and the impedance of T1 switch (which varies between 0.5 kΩ and 2.5kΩ) and can be expressed as:

$$\tau_{SSTARTmin}\,(\mathrm{ms}) = 0.5 * C_{cp1}\,(\mu\mathrm{F})$$

- Once PG state is reached (PG=1), SOFTST pin is disconnected from VDD and is floating. Ccp1 capacitor doesn’t influence the AC bandwidth of the feedback loop anymore and the system works at its nominal AC response.

For more information, please contact Cissoid.

LDO and Vref

The internal 2.5V voltage reference is used by the internal linear low-dropout voltage regulator (LDO) in order to provide the 5V supply (VDD) required by the CHT-MAGMA. This 5V supply requires an external decoupling capacitor for stability and noise reduction. It can provide some current to an external circuit (for example, provide the supply of an external driver).

Activation of PWMN signal

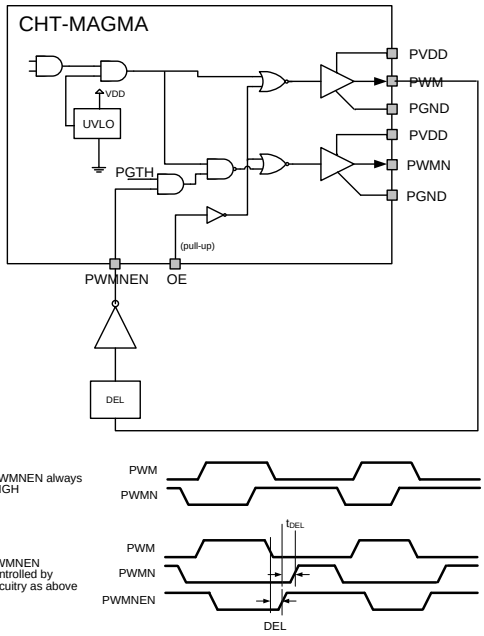
To have this output pin carrying the inverse (non-overlapping on rising PWM edge and overlapping on falling edge PWM) of PWM output pin, following conditions need to be met:

- PWMNEN signal should be connected to VDD
- PGTH signal should be connected to VDD; in this case, power good and soft-start functions are not available anymore

When one of those conditions is not met, PWMN logical level is “0”.

Generation of truly non-overlapped PWM and PWMN signals

As mentioned in previous paragraph, when PWMNEN is HIGH, PWMN pin carries the inverse of the PWM signal but with an overlap on falling PWM edge.
In some applications, designers may want to generate truly non-overlapped PWM and PWMN signals.
This can be achieved by driving the PWMNEN signal with the inverse of the PWM signal as described in figure below:



The non-overlap delay between falling PWM edge and rising PWMN edge is then the sum of:

- Internal t_{DEL} (refer to Typical Performance Characteristics section for definition and typical value)
- External invertor propagation delay
- Any additional delay (DEL box in the figure above) implemented eg with an RC network.

The external invertor can be implemented using either an SNMOS80 with a pull-up resistor or a CHT-7404.

The non-overlap delay between falling PWMN edge and rising PWM edge is fixed internally in the CHT-MAGMA device (refer to Typical Performance Characteristics section for definition and typical value)

Max duty cycle management

Typically, the max duty cycle is defined by the clock signal (CK) and can be configured (by means of external components) between 60 and 95%

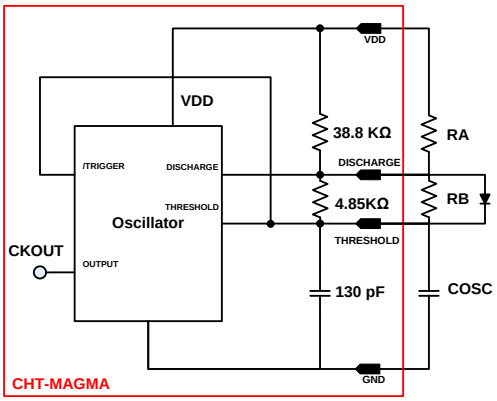
In some applications, the stability of the system is not guaranteed when duty cycles is above 50%. So it can be desirable to limit the duty cycle by design.

There are 2 ways to fix a duty cycle to less than 50%.

Method 1:

Since CHT-MAGMA oscillator is based on a 555 architecture, one can largely decouple Ton and Toff time generation by implementing a diode between DISCHARGE and THRESHOLD pins (see figure below). Ton and Toff times are then calculated as follows:

- Ton= 0.67*Ra*C
- Toff= 0.67*Rb*C



The main drawback of this solution is that it requires one additional external diode.

Method 2:

By making sure that SWT node reaches 5V after a duration equivalent to the max allowable duty cycle, the system will never generate any duty cycle higher than this maximum; indeed, the COMP signal has a dynamic range of [0-5]V and so once SWT node reaches 5V, whatever the value of the COMP signal, the “PWM” flip-flop will be reset.

This method only works if saw-thooth network supply voltage is sufficiently higher than 5V (min 9-10V).
When selecting the Rswt and Cswt component values, one needs to take into account following rules:

- SWT node is clamped down to ~0.9V (diode drop)
- Time to reach 5V can be computed assuming a linear behavior of the RC network

$$T = \frac{Cswt*(5V-0.9V)}{(Vin-1)/Rswt}$$

- Since there is an ESD diode between SWT and 5V internal supply, SWT node will be clamped to 5.7V and a current ([Vin-5.7V]/Rswt) will flow though this diode into the 5V internal supply; this current should be lower than 500µA to not charge the voltage regulator (which can not absorb current).

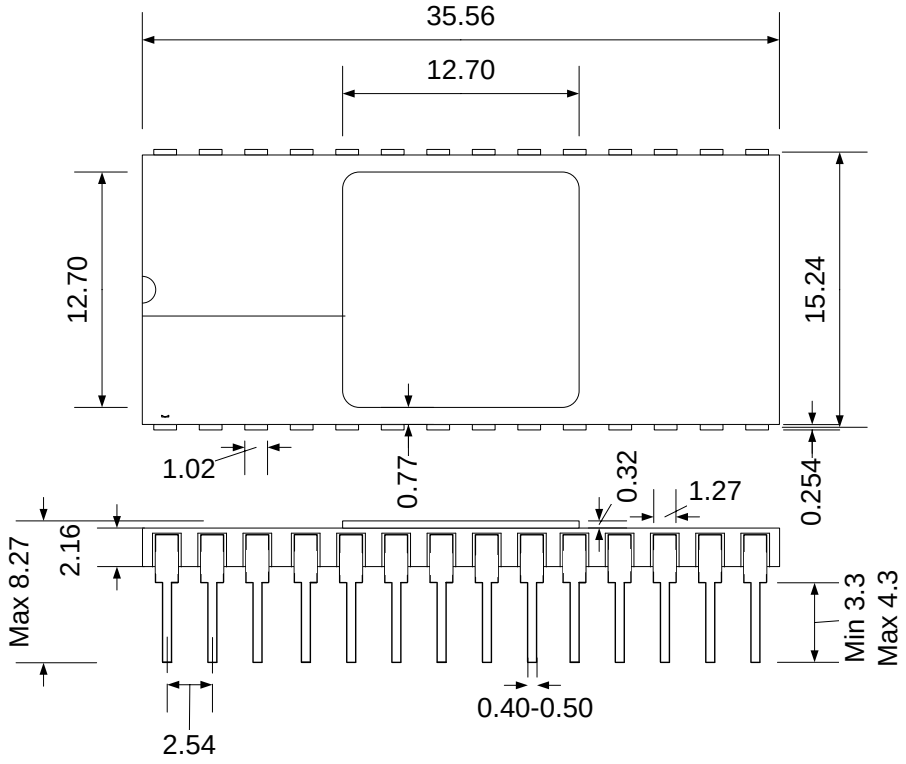
The main advantage of this method is that it does not require any additional external components but only a careful component value selection.
Please contact Cissoid for more information.

Application development
Cissoid recommends that in the application testing process, the power supply is gradually increased starting from 7V; at each step, presence of glitches should be checked. If any and if those glitches are close to the maximum operating conditions, the application should be reworked to decrease drastically the amplitude of those glitches before increasing further the power supply level.
Be aware as well that when using Magma in a loop, any loop instability can lead to signals exceeding max rating values

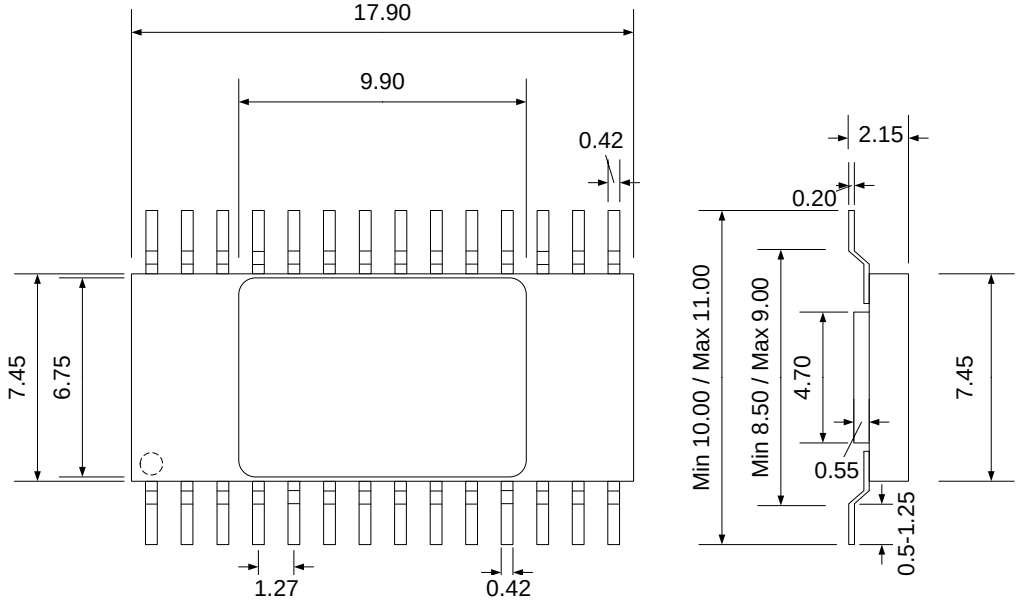
Ordering Information

Ordering Reference	Package	Temperature Range	Marking	STATUS
CHT-MAGMA-CDIL28-T	Ceramic DIL28	-55°C to +225°C	CHT-MAGMA	Not for new designs
CHT-MAGMA-CSOIC28-T	Ceramic SOIC28	-55°C to +225°C	CHT-MAGMA	Active

Package Drawing



CDIL 28 Drawing (mm +/- 10%)



CSOIC 28 Drawing (mm +/- 10%)

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 11 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: mailto:sales@cissoid.com
Sales Representatives:	**Visit our website:** http://www.cissoid.com/company/about-us/contacts.html

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