CHT-HADES2P
Datasheet

Version: 1.4
20-Dec-23
(Last Modification Date)

HighTemperature Gate Driver Primary Side IC: DC-DC Controller & Isolated Signal Transceivers

General description

CHT-HADES2P is a high-temperature, high reliability single chip primary side of a gate driver solution. It implements a current mode controlled DC-DC flyback converter for the generation of the on-board power supplies and the isolated data transmission from the external control interface to the 2 secondary sides and performs local fault management.
This device has been designed in a way to reduce as much as possible the required number of external passive devices and to limit the requirement in high capacitor values (large footprint at high temperature).
Its features a UVLO monitoring on the incoming power supply, a linear voltage regulator to generate the local 5V supply voltage and an on/off keying modulation of the data signal towards the secondary side.
It offers wide voltage range for the input PWM signals (5 to 15V) and hysteresis to enhance immunity to system noise; it also features a spike filtering function on those PWM signals to prevent spurious turn-on/turn-off of the secondary gate drivers.

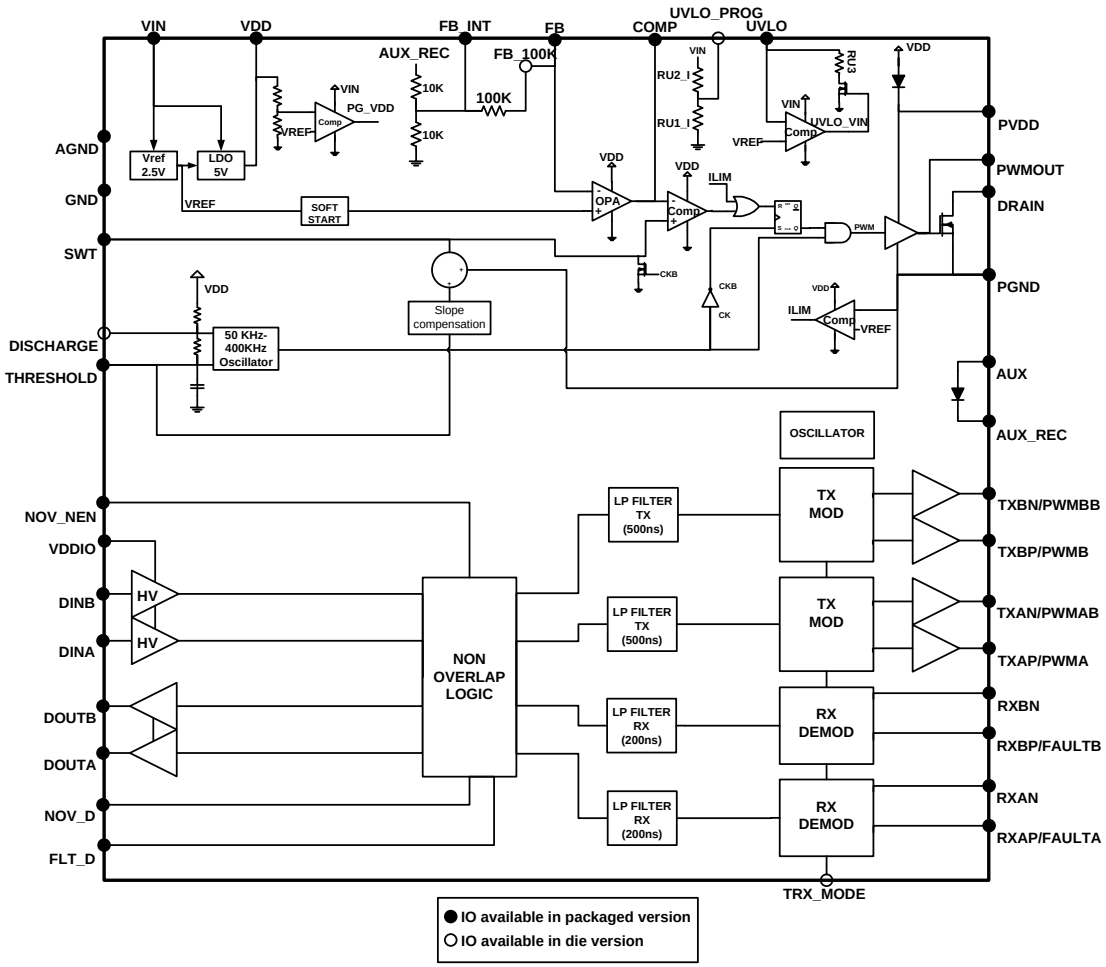
Applications

- Ideally suited for high reliability markets like automotive, aerospace, railways, Oil & Gas
- Motor drivers : down-hole, electrical cars, railways, industrial pumps, …
- DC-DC converters and SMPS : battery chargers, …
- Inverters : solar inverters, smart grid, EV and HEV, 3 phases inverters
- Power conversion : uninterruptible power supplies, wind turbine, …

Features

- Operating junction temperature:
  - from -55°C to +225°C
- Supply voltage: 10-16.5V
- Configurable Under-Voltage Lockout
- Integrated flyback DC-DC converter
  - typ. 180 kHz switching freq.
- Current mode control
- Cycle by cycle current limit
- Integrated switching transistor
  - Rdson: 0.8Ω typ.
- Optional external switching transistor
  - Integrated 3Ω typ. push-pull driver
- Configurable local non-overlap management
- Open-drain Dual Fault outputs
- High voltage Dual PWM inputs
- OOK modulated interface:
  - 2 TX and RX channels
- Data rate:
  - up to 2 Mbits/s per TX channel
- Propagation delay (TX):
  - typ. 40 ns
- TX jitter (RMS cycle-2-cycle) :
  - max 6 ns
- Hysteresis on PWM inputs
- Fault generation with programmable automatic re-start timer
- Configurable 500ns spike filter on PWM paths
- Common mode transient immunity:
  - > 50KV/µS typ.
- Package: CQFP32

Functional Block Diagram



Pin Description:

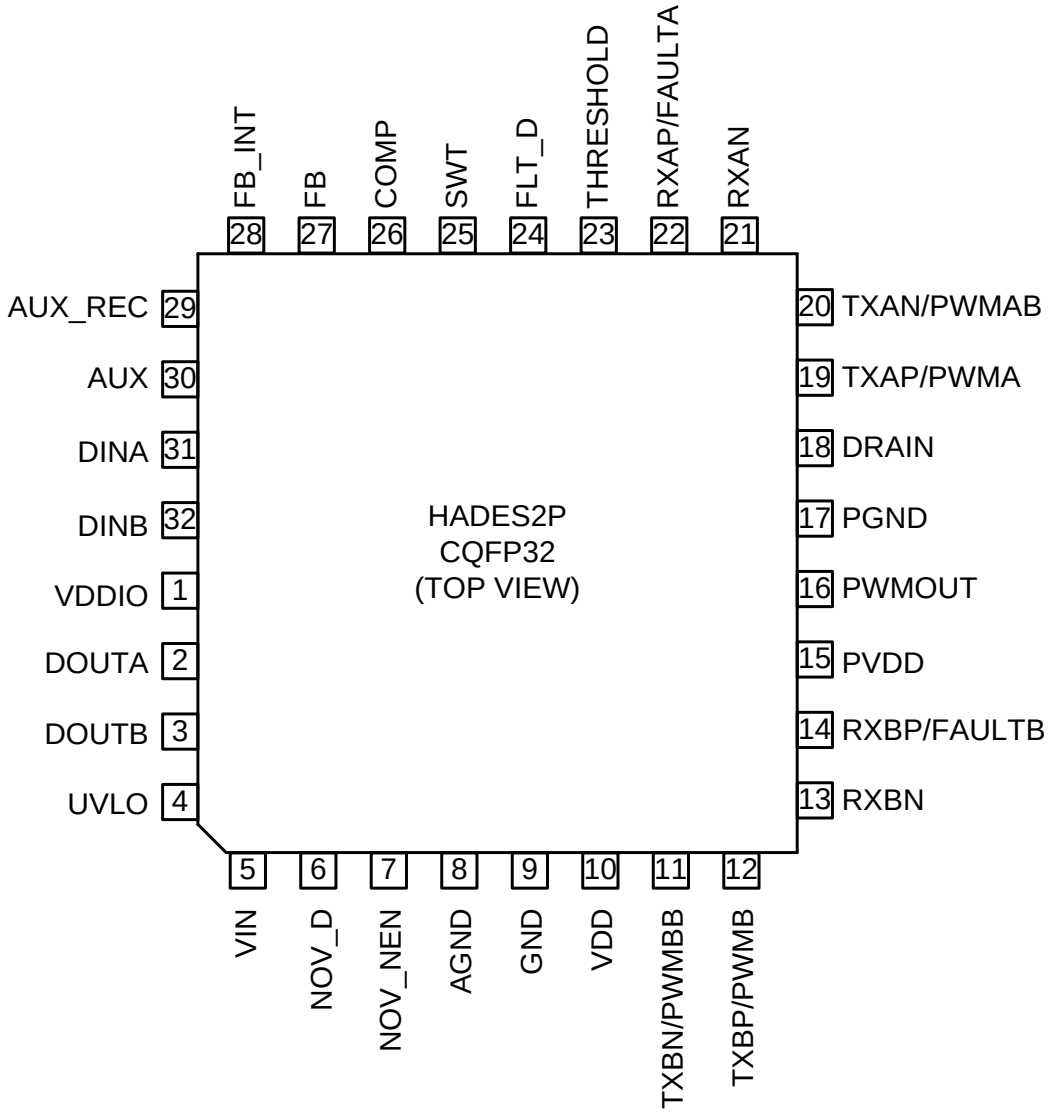
Pin #	Pin Name	Pin Description
1	VDDIO	Reference voltage for DINA/DINB high voltage inputs. Defines the maximum dynamic range of DINA/DINB pins
2	DOUTA	Open drain output of RX channel A
3	DOUTB	Open drain output of RX channel B.
4	UVLO	UVLO input pin (acting on “VIN-GND” signal)
5	VIN	Primary positive power supply; feeds internally bandgap, voltage regulator and DINA/DINB TX input buffers
6	NOV_D	Non-overlap delay programming. When non-overlap is disabled, input PWM filtering can be enabled by shorting NOV_D to VDD (internal 200kΩ pull-down present) .
7	NOV_NEN	Select between local non-overlap (“0”) and external non-overlap generation (“1”) (internal pull-up). When local non-overlap is selected, DINA is the input pin.
8	AGND	Analog negative power supply
9	GND	Negative power supply
10	VDD	5V positive supply of component core (output of internal voltage regulator)
11	TXBN/PWMBB	Negative differential output of TX channel B; to be connected to the primary of the transformer or Inverted PWM channel B digital output signal (push-pull)
12	TXBP/PWMB	Positive differential output of TX channel B; to be connected to the primary of the transformer or PWM channel B digital output signal (push-pull)
13	RXBN	Negative differential input of RX channel B; to be connected to the secondary of the transformer.
14	RXBP/FAULTB	Positive differential input of RX channel B; to be connected to the secondary of the transformer or FAULT channel B digital Schmitt trigger input
15	PVDD	Positive supply of DC-DC PWM driver stage; to be connected to an external bootstrap capacitor
16	PWMOUT	DC-DC PWM driver output
17	PGND	Negative supply of DC-DC PWM driver stage and source of switching transistor
18	DRAIN	Drain of switching transistor
19	TXAP/PWMA	Positive differential output of TX channel A; to be connected to the primary of the transformer or PWM channel A digital output signal (push-pull)
20	TXAN/PWMAB	Negative differential output of TX channel A; to be connected to the primary of the transformer or inverted PWM channel A digital output signal (push-pull)
21	RXAN	Negative differential input of RX channel A; to be connected to the secondary of the transformer.
22	RXAP/FAULTA	Positive differential input of RX channel A; to be connected to the secondary of the transformer or FAULT channel A digital Schmitt trigger input
23	THRESHOLD	Node of the internal oscillator. Reduce as much as possible parasitic capacitances on this node if the internal oscillator is used. Enables to change PWM frequency and duty cycle
24	FLT_D	Set the Fault reset delay. Connect capacitor to this pin to program delay; When fault has been detected, driver is turned-off for a period of time defined by FLT_D.
25	SWT	SawTooth signal. Leave unconnected at PCB level.
26	COMP	Output of the internal error amplifier & input of the PWM comparator
27	FB	Negative input of the error amplifier
28	FB_INT	Internal node of feedback network
29	AUX_REC	Rectified 5V output. Used as voltage feedback signal by DC-DC control loop
30	AUX	Non rectified auxiliary input
31	DINA	High voltage compatible Schmitt trigger input of TX channel A
32	DINB	High voltage compatible Schmitt trigger input of TX channel B

Pad Description (Available in die version):

Pad #	Pad Name	Pad Description
[1]	TRX_MODE	Select transmission mode towards secondary side (internal pull-down): “0”: modulated control interface “1”: standard digital interface (PWM/FAULT)
1	UVLO_PROG	Middle point of internal resistor divider fixing a default UVLO threshold Connect UVLO_PROG pad to UVLO pin to use this internal threshold; otherwise, leave open
1	FB_100K	Internal node of 100kHz switching frequency compensation network. Connect to FB pin if used, else leave unconnected
1	DISCHARGE	Node of the internal oscillator. Enables to change PWM frequency and duty cycle

[1] Cfr Die&Bonding instructions document

Pinout:


FB_INT 28
FB 27
COMP 26
SWT 25
FLT_D 24
THRESHOLD 23
RXAP/FAULTA 22
RXAN 21
AUX_REC 29
AUX 30
DINA 31
DINB 32
VDDIO 1
DOUTA 2
DOUTB 3
UVLO 4
HADES2P
CQFP32
(TOP VIEW)
20 TXAN/PWMAB
19 TXAP/PWMA
18 DRAIN
17 PGND
16 PWMOUT
15 PVDD
14 RXBP/FAULTB
13 RXBN
5 VIN
6 NOV_D
7 NOV_NEN
8 AGND
9 GND
10 VDD
11 TXBN/PWMBB
12 TXBP/PWMB

Absolute Maximum Ratings

Parameter	Min.	Max.	Units
(VIN-GND/AGND)	-0.5	18	V
(VDD-GND/AGND)	-0.5	6	V
(PVDD-PGND)	-0.5	6	V
(AUX_REC-GND/AGND)	-0.5	6	V
(AUX-AUX_REC)	-18	0.5	V
UVLO	-0.5	18	V
VDDIO	-0.5	18	V
DINA/DINB/DOUTA/DOUTB	-0.5V	18	V
TXAP/PWMA,TXAN/PWMAB TXBP/PWMB,TXBN/PWMBB RXAP/FAULTA,RXAN RXBP/FAULTB,RXBN NOV_NEN,NOV_D,THRESHOLD,FB,FB_INT COMP,SWT,FLT_D	-0.5V	6	V
PWMOUT	PGND-0.5V	6	V
DRAIN-PGND	-0.5	80	V
Junction Temperature		250	°C
ESD Rating (Human Body Model)	1.5		kV
Max supported power dissipation		2.5	W

Operating conditions

Parameter	Min.	Max.	Units
(VIN-GND/AGND)	10	16.5[2]	V
(VDD-GND/AGND)	4.75	5.25	V
(PVDD-PGND)	3.75	5.25	V
(AUX_REC-GND/AGND)	0	5	V
(AUX-AUX_REC)	-15	0.5	V
UVLO	0	VIN	V
VDDIO	VDD	VIN	V
DINA/DINB/DOUTA/DOUTB	GND	VIN	V
TXAP/PWMA,TXAN/PWMAB TXBP/PWMB,TXBN/PWMBB RXAP/FAULTA,RXAN RXBP/FAULTB,RXBN NOV_NEN,NOV_D,THRESHOLD,FB,FB_INT COMP,SWT,FLT_D	GND	VDD	V
PWMOUT	PGND	PVDD	V
DRAIN-PGND	0	80	V
Junction Temperature		225	°C
Max supported power dissipation[3]		2	W

Parameter	Condition	Min	Typ	Max	Units
Thermal resistance					
$R_{\Theta JA}$: junction–to-air thermal resistance	Mounted on PCB; no thermal pad at PCB level; still air; devices in horizontal or vertical position		40		°C/W

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

[2] For use at higher input voltage, contact CISSOID

[3] Please refer to section Power dissipation on page 23 for more information

Electrical Characteristics

Unless otherwise stated: (VIN-GND)=15V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
External Power Supply					
External Power Supply VIN	Versus GND	10		16.5[4]	V
I_{AVG}(VIN)	DC-DC operational F_s = 180 kHz DINA=DINB= 20 kHz 50% duty cycle signal VIN-GND = 15V No fault situation		16.7		mA
	DC-DC operational F_s = 180 kHz DINA=DINB= 0 VIN-GND = 15V No fault situation		7.4		mA
	Fault at Primary and secondary's		2.4		mA
	Fault at secondary's		4.5		mA
Under-voltage Lockout (UVLO)					
UVLO minimum level		**7**			V
UVLO comparison thresh-old		2.424	2.525	2.626	V
UVLO threshold variation with temperature			-0.6		mV/°C
UVLO hysteresis resistor		**134.1**	185	**228.5**	kΩ
Default UVLO High level	With internal resistors Only available with die version		9.6		V
Default UVLO Low level			7.8		V
Delay from UVLO detection to DOUT @ fault level			160		ns
5V Power Supply					
Internal 5V Power Supply (VDD) versus VSS	(VIN-VSS) from 10V to 16.5V, Iout from 0.25mA to 50 mA	**4.8**	5.05	**5.3**	V
Output Capacitor C_{VDD}	Capacitor value at Tamb=225°C	**1000**			nF
Output Current	20mA consumed by the device in normal operation	**2.5**		**50**	mA
Initial Accuracy	(VIN-GND)= 15V; Iout=2.5mA		+/-2		%
Drift with temperature	(VIN-GND)= 15V; Iout=2.5mA		-1		mV/°C
Line Regulation	(VIN-GND) from 10V to 16.5V; Iout=13mA		+/-0.2		%
Load Regulation	(VIN-GND)= 15V; Iout from 2.5mA to 50mA		-0.6		%
Power-Good threshold	Falling edge, relative to nominal Rising edge, relative to nominal		80 90		%
Internal voltage reference (VREF) (seen on FB node, including OPA offset)					
Initial Accuracy	Tj=25°C; Vin=15V	2.475 -2	2.525	2.575 +2	V %
Temperature drift		**-900**	-600	**-50**	µV/°C
Line regulation	VIN from 10V to 16.5V		-0.16		mV/V

[4] For use at higher input voltage, contact CISSOID

Electrical Characteristics (continued)

Unless otherwise stated: (VIN-GND)=15V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

TRX_MODE =0					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Units**
Input signal (RXP/FAULT,RXN)					
Impedance	Between RXP & RXN/GND Between RXN & RXP/GND	**3.03**	3.43	**3.83**	kΩ
Common mode transient immunity	0.5 pF pulse transformer parasitic capacitance	**50**			KV/µS
Output signals (TXP/PWM, TXN/PWMB)					
High state output resistance			20		Ω
Low state output resistance			23.5		Ω
Modulation frequency			14.5		MHz
Modulation frequency variation	Includes process/ temperature/power supply variations	**-35**		**+40**	%
Modulation frequency duty cycle		**48.5**		**51.5**	%
DOUTA/DOUTB open drain outputs					
On resistance	Applies to DOUTA/DOUTB			**30**	Ω
Min pull-up resistance		**300**			Ω
Output Fall Time (90% to 10%)	On 50 pF external capacitor Pull-up: 300 Ohm to VIN		36		ns
DINA/DINB inputs					
VDDIO reference voltage input impedance			80		kΩ
HIGH voltage threshold for digital inputs	Applies to DINA, DINB	**0.6* VDDIO**	2/3* VDDIO	**0.73* VDDIO**	V
LOW voltage threshold for digital inputs	Applies to DINA, DINB	**0.28* VDDIO**	1/3* VDDIO	**0.42* VDDIO**	V
Hysteresis			1/3* VDDIO		V
Input impedance	Wrt to GND	**47**			kΩ
NOV_NEN/NOV_D (when used as input)					
Minimum HIGH level input voltage V_{IH}		**VDD-0.5V**			V
Maximum LOW level input voltage V_{IH}				**0.5V**	V
Non-overlap delay (NOV_D)					
Non Overlap delay range	C_{NOV_D} from 30pF to 500pF	**0.2**		2.75	µs
Non-Overlap delay accuracy	Not taking into account variation of external capacitor	**-36**		**54**	%

Fault data path					
Propagation delay (RXP/RXN →DOUT)	Modulated transmission interface		400		ns
PWM data path					
Data rate				**2000**	kbps
Duty cycle		**0**		**100**	%
DIN spike filter delay		**310**	500	**760**	ns
DIN spike pulse width distortion		**-106**	0	**87**	ns
Propagation delay (DIN →TXN/TXP)	Modulated transmission interface 500ns filter not active		40		ns
Jitter (RMS cycle-2-cycle)	On PWM rising edge			**0.3**	ns
Jitter (RMS cycle-2-cycle)	On PWM falling edge			**6**	ns
Fault latching time					
Timer range t_{FLT_D}	C_{FLT_D} from 20pF to 1µF	**0.01**		**500**	ms
Timer variation	C_{FLT_D} = 20 nF; excluding external capacitor spread	**7.2**	10	**12.5**	ms

Electrical Characteristics (continued)

Unless otherwise stated: (VIN-GND)=15V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

TRX_MODE =1 (Only available for the die version)					
Parameter	**Condition**	**Min**	**Typ**	**Max**	**Units**
Input signal (RXP/FAULT)					
Input start threshold		**3.03**	3.43	**3.83**	V
Input stop threshold		**1.1**	1.39	**1.85**	V
Hysteresis		**1.68**	2.04	**2.39**	V
Output signals (TXP/PWM, TXN/PWMB)					
Minimum HIGH level output voltage V_{OH}	IOH < 8mA (source)	**4.4**			V
Maximum LOW level output voltage V_{OL}	IOl < 8mA (sink)			**0.63**	V
Output Rise/Fall Time (10% to 90%)	On 50 pF external capacitor		10		ns
DOUTA/DOUTB open drain outputs					
On resistance	Applies to DOUTA/DOUTB			**30**	Ω
Min pull-up resistance		**300**			Ω
Output Fall Time (90% to 10%)	On 50 pF external capacitor Pull-up: 300 Ohm to VIN		36		ns
DINA/DINB inputs					
VDDIO reference voltage input impedance			80		kΩ
HIGH voltage threshold for digital inputs	Applies to DINA, DINB	**0.6* VDDIO**	2/3* VDDIO	**0.73* VDDIO**	V
LOW voltage threshold for digital inputs	Applies to DINA, DINB	**0.28* VDDIO**	1/3* VDDIO	**0.42* VDDIO**	V
Hysteresis			1/3* VDDIO		V
Input impedance	Wrt to GND	**47**			kΩ
NOV_NEN/NOV_D (when used as input)					
Minimum HIGH level input voltage V_{IH}		**VDD-0.5V**			V
Maximum LOW level input voltage V_{IH}				**0.5V**	V
Non-overlap delay (NOV_D)					
Non Overlap delay range	C_{NOV_D} from 30pF to 500pF	**0.2**		2.75	µs
Non-Overlap delay accuracy	Not taking into account variation of external capacitor	**-36**		**54**	%
Fault data path					
Propagation delay (RXP→ DOUT)	Digital RX interface		250		ns
PWM data path					
Data rate				**2000**	kbps
Duty cycle		**0**		**100**	%
DIN spike filter delay		**310**	500	**760**	ns
DIN spike pulse width distortion		**-106**	0	**87**	ns
Propagation delay (DIN →TXN/TXP)	Digital TX interface 500ns filter not active		40		ns
Fault latching time					
Timer range t_{FLT_D}	C_{FLT_D} from 20pF to 1µF	**0.01**		**500**	ms
Timer variation	C_{FLT_D} = 20 nF; excluding external capacitor spread	**7.2**	10	**12.5**	ms

Electrical Characteristics (continued)

Unless otherwise stated: (VIN-GND)=15V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Switching transistor					
On resistance	VGS=5V,25°C		0.8		Ω
	VGS=5V,225°C		1.6		Ω
Breakdown voltage	VGS=0V, 225°C	**80**			V
Peak pulsed drain current	25°C		4		A
	225°C		2		A
Drain leakage current	25°C		10		nA
	225°C		11		uA
Average current				**0.5**	A
Input capacitance (C_{ISS})	VGS =0VDC; VDS =80VDC; f= 1MHz		232		pF
Output capacitance (C_{OSS})			38		pF
Feedback capacitance (C_{RSS})			9.8		pF
Total switching energy (Turn-on + Turn-off)	V_{DS} =40V; ID= 1A; 25°C		413		nJ
PWMOUT output					
Output resistance			3		Ω
Maximum load capacitance				**2**	nF
Duty Cycle		**0**		D_{CK}	%
OPA					
Output voltage swing	Tj=25°C, IOUT = 1mA	0.5		VDD-0.5	V
Output current	Tj=25°C		1		mA
DC gain	Tj=25°C Tj=225°C		100 87		dB dB
Gain-bandwidth product	Cload=30pF	**1.3**	1.5		MHz
Slew rate	Cload=30pF	1.0	1.2	1.7	V/µs
Phase margin	Cload=30pF	**50**	>60		Degree
Input leakage current (“FB” pin)	In packaged part version, 100K resistor is connected to FB pin			**±10**	nA
Soft Start					
Reference soft start			2		ms
Internal DC-DC oscillator					
Frequency[5]	THRESHOLD pad disconnected	**110**	181	**276**	kHz
Max Duty cycle D_{CK}	THRESHOLD pad disconnected Based on internal R/C values	**88**	90	**92**	%
Frequency drift with temperature	THRESHOLD pad disconnected		0.15		kHz/°C
Adjustable frequency range		50		400	kHz
Adjustable duty cycle		60		95	%
RA_I and RB_I temperature coefficient			-860		ppm/°C
RA_I and RB_I absolute variation		-28		24	%
COSC_I temperature coefficient			23		ppm/°C
COSC_I absolute variation		-15		23	%
Current limit					
Current limit threshold	Rshunt = 0.5Ω	1	1.2	1.42	A
Current limit delay			100		ns
Current limit blanking time		315	500	760	ns
Current sensing resistor					
Rshunt		**0.49**	0.5	**0.51**	Ω
AUX rectification diode					
Reverse breakdown voltage		**18**			V
Reverse leakage	Tj=25°C		2		nA
	Tj=225°C		1.2		uA
Forward voltage	I_{fw} = 1mA		0.73		V

[5] As the internal oscillator capacitor (COSC_I) is only 145pF, any additional parasitic capacitors on pins “THRESHOLD” and “DISCHARGE” can decrease the oscillation frequency.

Typical Performance Characteristics

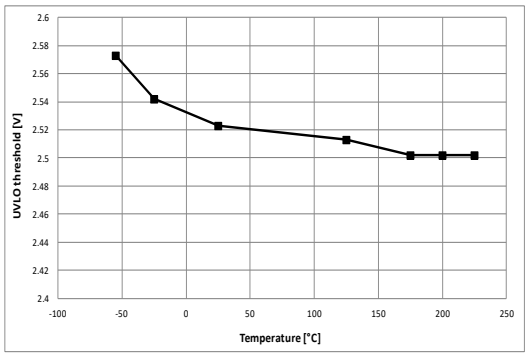


Figure 1. UVLO threshold

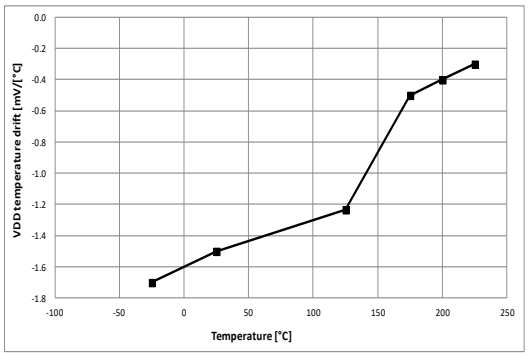


Figure 2: Voltage regulator temperature drift (VIN=15V, Iout = 15mA)

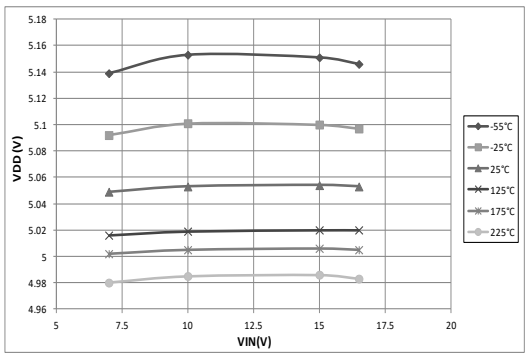


Figure 3: Voltage regulator line regulation (Iout =3 mA)

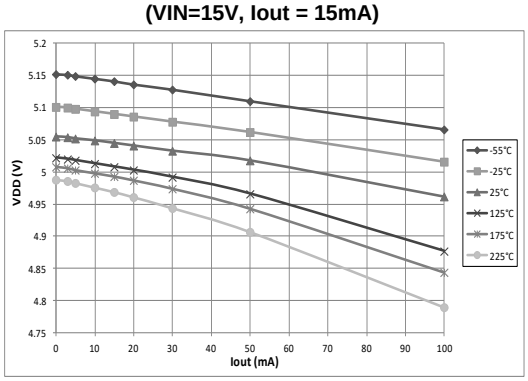


Figure 4: Voltage regulator load regulation (Vin=15V)

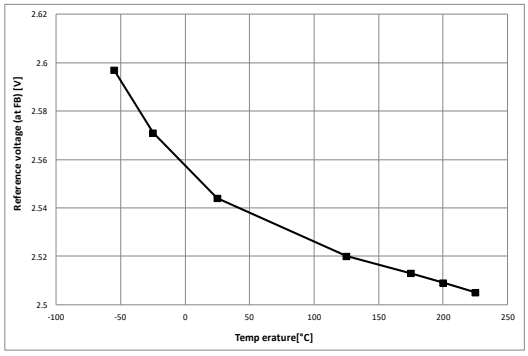


Figure 5: Voltage reference @ FB pin (including OPA offset)

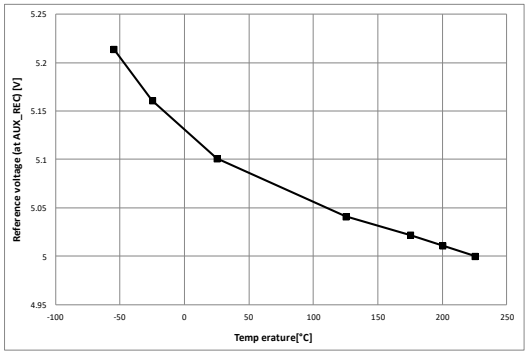


Figure 6: Voltage reference @ AUX_REC pin (including OPA offset and AUX_REC divider)

Typical Performance Characteristics (continued)

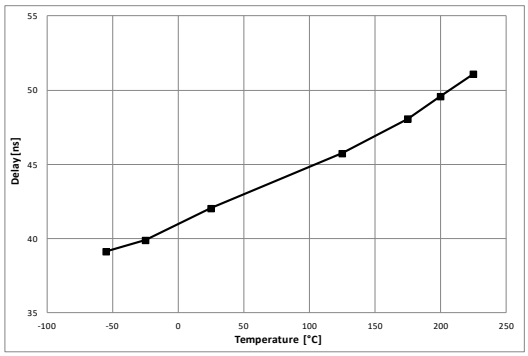


Figure 7: DIN => TX Propagation Delay (modulated interface)

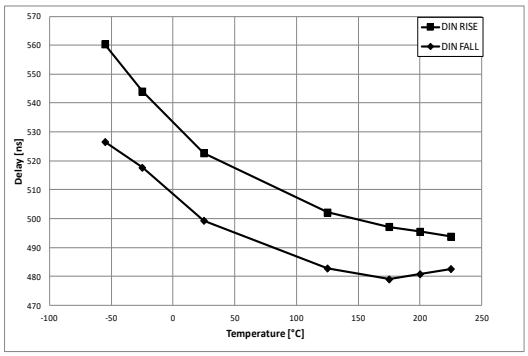


Figure 8: DIN->TX Propagation Delay (modulated interface; spike filter on)

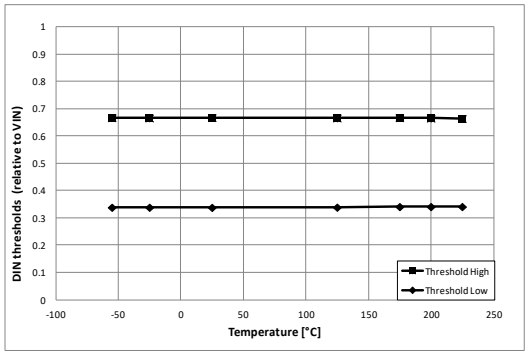


Figure 9: DIN Hysteresis thresholds (relative to VIN=15V)

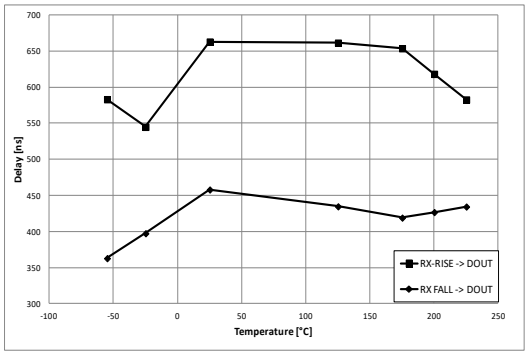


Figure 10: RX => DOUT Propagation Delay vs. Temperature (modulated interface)

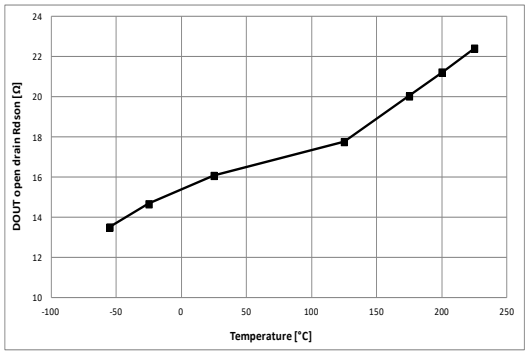


Figure 11: DOUT open drain Ron (VIN=15V)

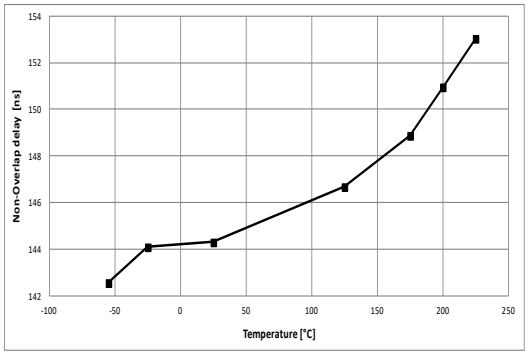


Figure 12: Non-Overlap delay (no external capacitor)

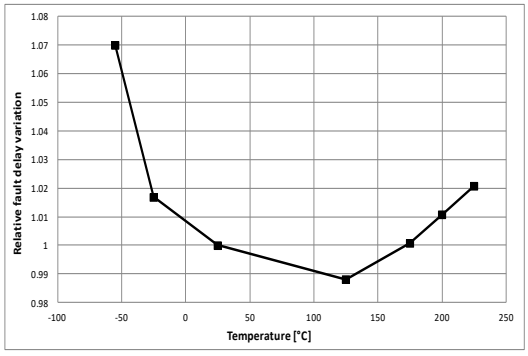


Figure 13. Fault timer tFLT_D (CFLT_D=20nF).

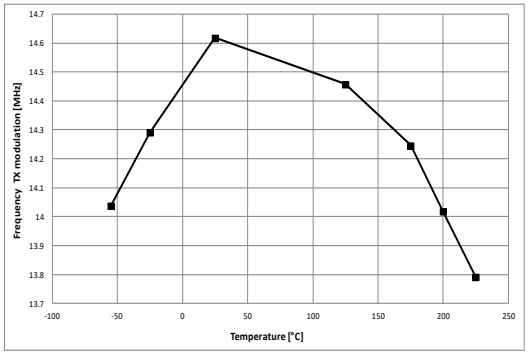


Figure 14: TX oscillator modulationfrequency

Typical Performance Characteristics (continued)

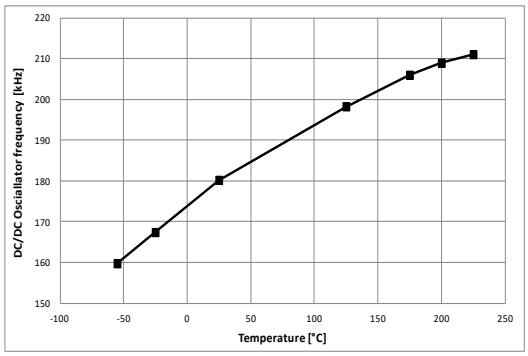


Figure 15: DC-DC oscillator frequency

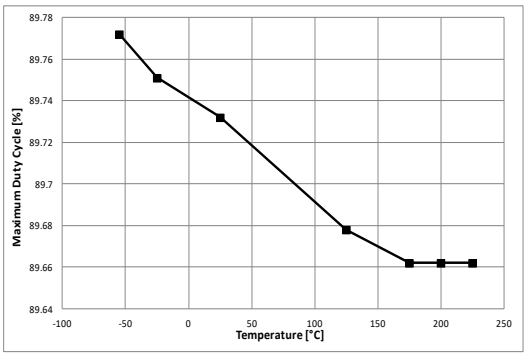


Figure 16: DC-DC Clock Duty Cycle

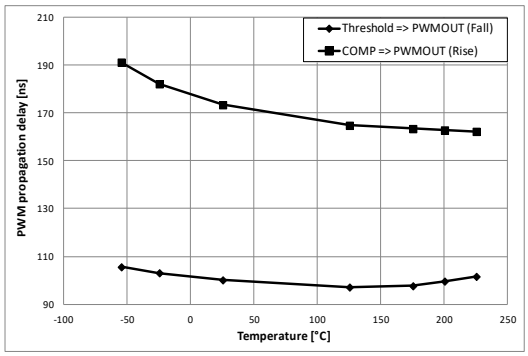


Figure 17. PWM Propagation

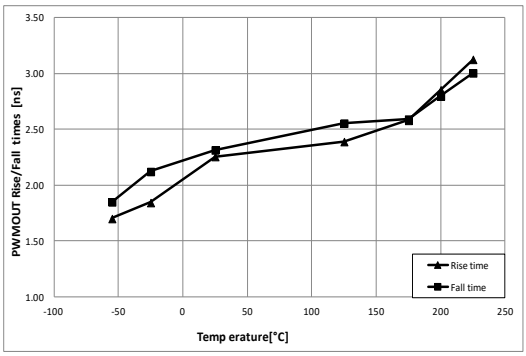


Figure 18. PWMOUT Rise/Fall times (No external load)

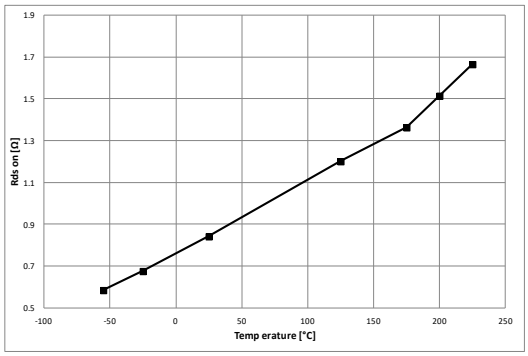


Figure 19: Switching transistor Ron

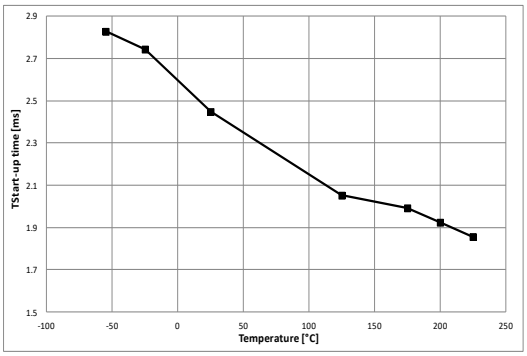


Figure 20: Soft start time

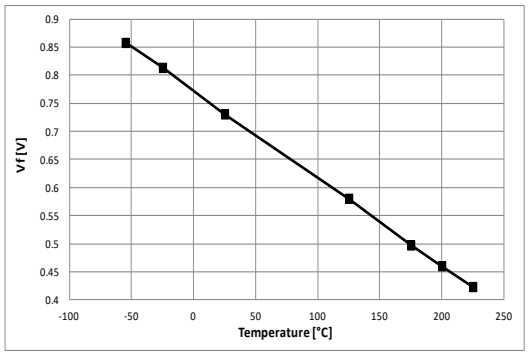


Figure 21: AUX diode Vf (If=1mA)

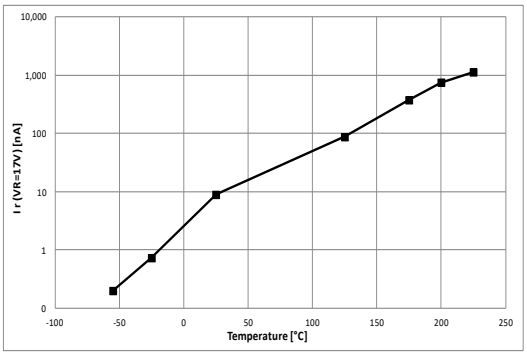


Figure 22: AUX diode Ir (Vr=17V)

Typical Performance Characteristics (continued)

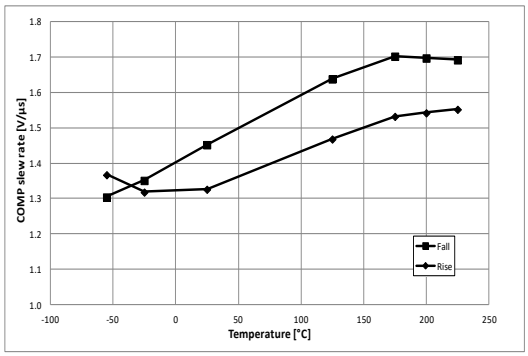


Figure 23. OPA Slew Rate

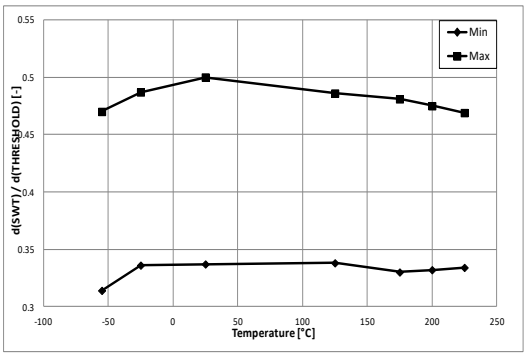


Figure 24. Voltage ramp gain/linearity

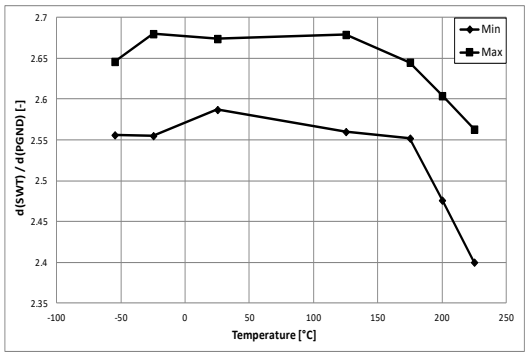


Figure 25. Current ramp gain/linearity

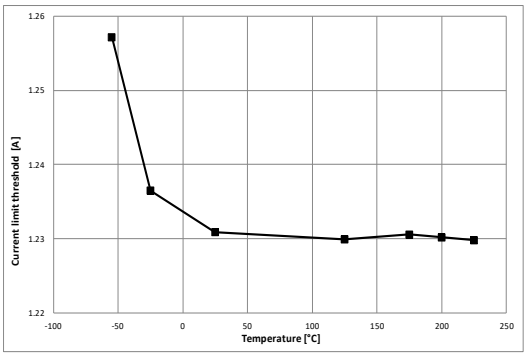


Figure 26. Current limit threshold (Rshunt = 0.5Ω)

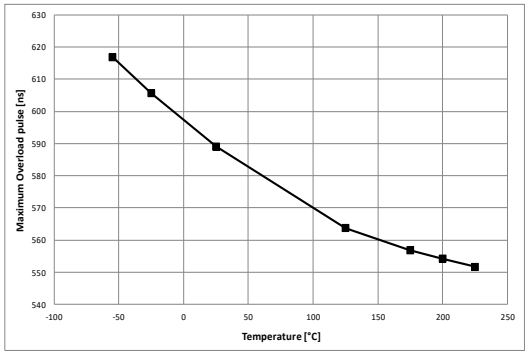


Figure 27 Maximum Overload Pulse Duration

Typical Performance Characteristics (continued)

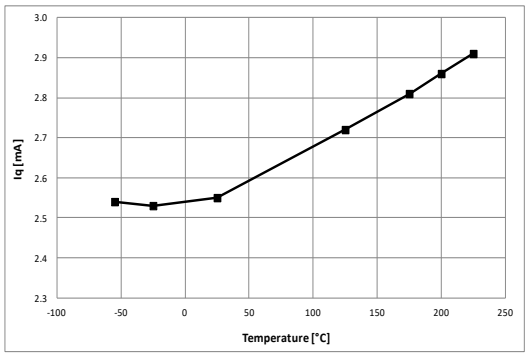


Figure 28. Average current VIN
(Primary and both Secondary's in fault; VIN=15V)

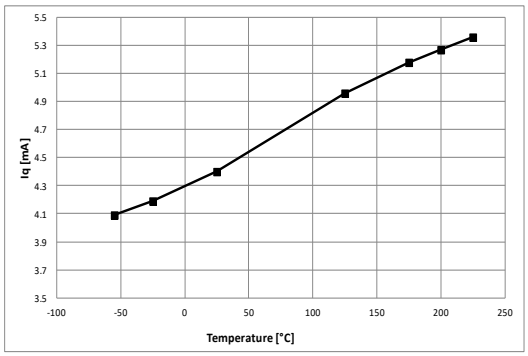


Figure 29. Average current VIN
(both Secondary's in fault; VIN=15V)

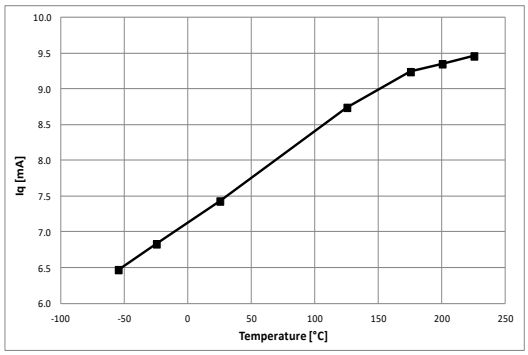


Figure 30. Average current VIN
(no fault, DINx=0; VIN=15V)

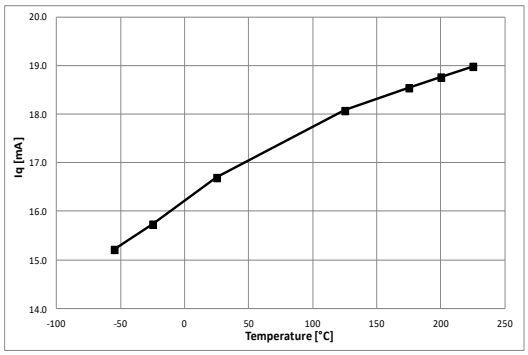


Figure 31. Average current VIN
(no fault, DINx=20kHz 50% DC; VIN=15V)

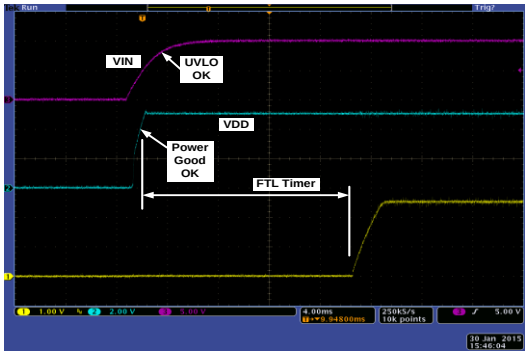


Figure 32. Start-up screen shot

Circuit functionality

General description

HADES2P is a high-temperature, high reliability, single-die gate driver primary side management. Its main features are:

- Fully integrated flyback DC-DC converter
- Integrated DC-DC 0.8Ω switching transistor; optionally, it provides a PWM output to drive an external transistor for higher power applications
- Cycle-by-cycle current limit
- Internal 5V voltage regulator powering internal logic and also usable to supply external 5V devices
- Permanent and programmable Under-Voltage Lockout (UVLO) monitoring on power supply
- Isolated data transmission (robust to high dV/dt) (data and fault) towards secondary side
- Digital 5V interface for data and fault (as alternative to isolated data transmission interface)
- Programmable fault timer with automatic restart
- Safe start-up sequence through monitoring of the main supply (UVLO) and of the voltage regulator output (through Power-Good function)
- High voltage compatible, Schmitt trigger IOs towards external controller
- Support of 2 separate incoming PWM channels and of locally generated non-overlapped PWM signals
- Configurable 500ns spike filter on incoming PWM signal for enhanced noise robustness

Under-Voltage Lockout (UVLO)

The aim of this function is to allow the user to specify a threshold voltage for the power supply under which the DC-DC is shut down and a fault is reported. The monitored power supply is “VIN-GND”.

The UVLO threshold is defined by means of 2 external resistors (RU1, RU2) connected to the pin UVLO (cfr Figure 33).

To avoid oscillation when (VIN-GND) is close to the UVLO threshold, a hysteresis is implemented internally via a resistor RU3 (shunting RU1 resistor before threshold high is reached).

UVLO thresholds are defined by the following equation:

$$\text{UVLO THR LOW} = 2.5V * \left(\frac{RU2+RU1}{RU1}\right)$$

$$\text{UVLO THR HIGH} = 2.5V * \left(\frac{RU2+(RU1*RU3)/(RU1+RU3)}{(RU1*RU3)/(RU1+RU3)}\right)$$

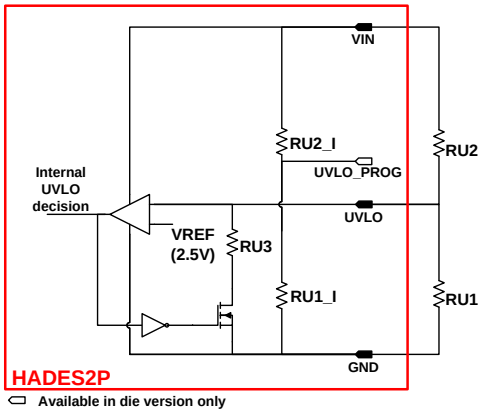


Figure 33: UVLO detection function

In the die version of HADES2P, integrated RU1_I/RU2_I offers following default values:

UVLO THRESHOLD HIGH = 9.6V

UVLO THRESHOLD LOW = 7.8V

Refer to the Fault management chapter for details about fault behavior and management.

Voltage reference and voltage regulator

HADES2P device includes on-chip voltage reference (2.5V) generator and also a voltage regulator providing 5V power supply (VDD).
The 5V supply is used internally by the transmission interface, the control logic, the DC-DC control loop HW (OPA, comparator, logic) and the PWMOUT predriver; it can be used to feed external devices as long as max current capability of the voltage regulator is not exceeded.

A Power-Good function monitors the voltage regulator output (VDD) (threshold: typ. 80% of VDD); the Power-Good information is used by the device state machine to control the device behavior.

The 2.5V reference voltage is used as reference voltage by the DC-DC function.

Those two functions are supplied by the VIN pin. A low-pass filter needs to be implemented on PCB between the main Vin (feeding the DC-DC flyback transformer) and HADES2P VIN pin to filter out the high DC-DC switching noise
(cfr Device power supplies and decoupling scheme section for more details).

Interface towards secondary

HADES2P offers two types of interface towards the secondary:

- Standard 5V digital interface: PWM (output), FAULT (input)
- Modulated transmission interface enabling transmission over isolation barrier through pulse transformers.

Pad “TRX_MODE” defines mode of operation (in packaged version, “TRX_MODE” is set “0” by an integrated pull-down on TRX_MODE pad):

- “0”: Modulated transmission interface
- “1”: Standard 5V digital interface

Modulated transmission interface is fully compatible with HADESV1 chipset and specifically with RHEA device (CHT-TIT4750).

The modulated transmission interface behaves as follows:

- the TX-MOD block uses an internally generated clock to modulate the internal PWM signal (using OOK modulation scheme) and to generate 2 complementary outputs. The 2 outputs drive the primary side of the pulse transformer in a differential manner.
- the RX-DEMOD block amplifies and demodulates the 2 signals from the transformer secondary side to generate an internal FAULT signal.

Two independent transmit and two independent receive channels are implemented enabling the support of high and low side secondary’s with a single HADES2P device.

External pulse transformers are used to transmit the information between primary and secondary.

The pulse transformer design has to cope with following constraints:

- Minimize parasitic capacitance (Cp) between Primary and Secondary; ideally Cp should be lower than 0.5 pF to meet 50KV/µs dV/dt robustness)
- Respect isolation requirements
- Primary inductance: 8 µH typ.
- Maximum current on primary side of 20 mA (HADES2P drive capability)
- Maximum signal frequency: 15 MHz
- Secondary to primary ratio of about 1.1 (ideally 1 but needs to be slightly higher to compensate transformer losses)

Detailed information on the pulse transformer design is available in the EVK-HADES1210 application note.

PWM&FAULT datapath

In the default configuration (through integrated pull-up on NOV_NEN pin), the 2 PWM datapaths are fully independent.

By pulling NOV_NEN pin down, it is possible to work with only 1 PWM signal and to have HADES2P generating the 2nd PWM signal with the proper non-overlap. The non-overlap t_{NOV_D} delay is implemented

and adjusted by an external capacitor C_{NOV_D} connected to the NOV_D pin and can be calculated as follows:

$$t_{NOV\_D}\ (ns) = 5.5 * C_{NOV\_D}(pF)$$

The duty-cycle of the PWM signals has an influence on the value of the non-overlap delay. This is reflected in the figure below.

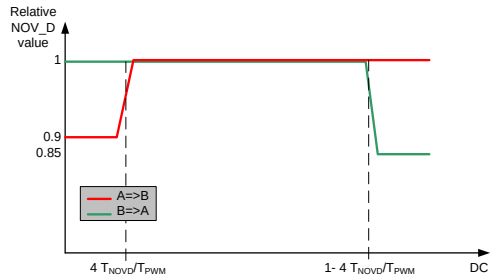


Figure 34: Non-Overlap delay variation wrt to PWM duty cycle (DC)

In case large perturbations would be expected on PWM input signals, it is possible to activate an internal spike filtering function suppressing any spike shorter than typ. 500ns. This is obviously increasing the propagation delay of the datapath.

If a fault occurs at the primary side, PWM internal signal will be forced to “0” as long as the fault is present. When the fault is cleared, external PWM signal will be propagated again through HADES2P on the next positive edge of the PWM external signal.

Table 1 illustrates the different options with respect to non-overlap management.

NOV_NEN	DINA	DINB	NOV_D	
0	Carries external PWM signal	X	Output pin	Connect to external capacitor to generate the local non-overlap time
1	Carries external PWM signal	Carries external PWM signal	Input pin	‘0’: no spike filter applied on DINA/DINB
1	Carries external PWM signal	Carries external PWM signal	Input pin	‘1’: spike filter applied on DINA/DINB

Table 1: PWM non-overlap programming

Whne using the mode “NOV_NEN= 0”, it is important that the PWM path “DINA => TXAP/TAXN” is driving the high-side transistor of the half-bridge; indeed, when DINA will be equal to “0” (meaning no action expected at power stage level), it is essential that high-side power transistor is turned off.

The 2 FAULT paths are fully independent. After the RX demodulation block, a 200ns low-pass filter is implemented; its function is to suppress potential glitches due to dV/dt event and so increase significantly the robustness to dV/dt.

A fault detected locally inside HADES2P device (please refer to FAULT management chapter) will force both fault signals (DOUT pins) to the FAULT level.

In case at system level, only one fault signal would be required, this function can easily be obtained by connecting the two DOUT pins together. Indeed, the HADES2P fault state implies DOUTx = “0” and so when connecting the two DOUT open-drain pins together, an ORing is performed (fault on any channel is generating an external fault signal).

At HADES2P start-up (before any internal logic is operational), special care has been taken to force DOUTx signal to “0” (fault state) till HADES2P reaches the normal state.

Table 2 and Table 3 provide the truth table of respectively PWM and FAULT datapaths.

DINx	RXxP/RXxN	Internal fault	TXx P	TXx N
0	MM[7]	0	0	0
1	MM	0	MM[6]	MM

Table 2: PWM datapath truth table

Modulated transmission interface		
RXxP/RXxN	Internal primary fault	DOUT
MM[7]	0	1
MM	1	0
0	0	0
0	1	0

Standard 5V interface		
RXxP/FAULT	Internal primary fault	DOUT
1	0	1
1	1	0
0	0	0
0	1	0

Table 3: FAULT datapath truth tables

DIN input buffer

The DIN input buffer offers the flexibility to support DIN signal voltage swings between 5V and VIN. This feature is especially useful when HADES2P is used in environments where increased noise immunity is required. This is achieved by setting VDDIO to a reference voltage corresponding to the max DIN expected amplitude e.g. 5V if DIN max high voltage is 5V or 15V if DIN max high voltage is 15V. Internally, the detection thresholds are adapted accordingly to 1/3 and 2/3 of the VDDIO signal value. A hysteresis of 0.33*VDDIO is implemented providing additional robustness on the signal path.

DOUT output buffer

The output buffer operates as an open-drain driver with a low Ron resistance (typ. 15Ω), enabling the use of low value pull-up resistor for increased noise immunity.

Fault management

In HADES2P device, fault is generated by any of those situations:

- Main power supply (VIN) is below the UVLO threshold
- VDD (linear voltage regulator output) is below the internal Power Good level

Those faults are internally combined to generate a unique fault signal. This internal fault signal is latched for a programmable period of time defined by an external capacitor connected to the pin FLT_D.

While the fault is latched:

- Both DOUT pins are tied to “0”
- TXAP/TXAN, TXBP/TXBN are tied to “0”
- DC-DC is off

After the predefined latch period of time, HADES2P circuit will attempt to return to normal operation:

- If the fault is still present, HADES2P will stay in that fault state till the fault disappears
- If the fault disappeared (e.g. temporary UVLO situation), HADES2P will go out of FAULT state and return to normal operation (DC-DC turned on and data paths active); still, on the PWM path, transition to normal operation will happen on the next positive edge of the incoming DINx signal.

The internal timer t_{FLT_D} value is implemented and adjusted by an external capacitor C_{FLT_D} connected to the FLT_D pin and its value can be calculated as follows:

$$t_{FLT\_D}\,(\mu s) = 0.5 * C_{FLT\_D}\,(pF)$$

[6] « MM » : modulated signal sent on both TXxP/TXxN pins

[7] « MM » : modulated signal received on both RXxP/RXxN pins

This primary fault signal will be combined with the faults returned by the secondary devices according to Table 4.

Prim fault	SecA fault	SecB fault	DOUTA	DOUTB
No	No	No	No fault	No fault
No	Yes	No	Fault	No fault
No	No	Yes	No fault	Fault
No	Yes	Yes	Fault	Fault
Yes	Yes or No	Yes or No	Fault	Fault

Table 4: FAULT aggregation table

Device start-up

Special care has been taken to provide to the device a deteministic behavior during power supply ramp-up.

Table 5 summarizes the different states in which the device can be and how the device behaves in each of those states.

VIN-GND < 4V	Internal bandgap is not operational yet	VDD (internal regulator output):“0V” PWMOUT: “0V” DRAIN: “HiZ” TXAP/TXAN, TXBP/TXBN: “0” DOUTA/DOUTB: “0” HADES2P in FAULT state
VIN-GND >4V & VIN-GND < 7V	Internal bandgap is operational Power good level not yet reached on VDD	PWMOUT: “0V” DRAIN: “HiZ” TXAP/TXAN, TXBP/TXBN: “0” DOUTA/DOUTB: “0” HADES2P in FAULT state
VDD >Power Good & VIN-GND < UVLOH-TH	Internal bandgap is operational Power good level reached on VDD UVLO threshold not yet reached on VIN	PWMOUT: “0V” DRAIN: “HiZ” TXAP/TXAN, TXBP/TXBN: “0” DOUTA/DOUTB: “0” HADES2P in FAULT state
VDD >Power Good & VIN-GND > UVLOH –TH	All functions OK	Normal device operation

Table 5: Start-up device behavior

DC-DC converter

HADES2P circuit integrates a voltage and current mode PWM DC-DC controller. The different blocks shown in the functional block diagram are described hereafter.

Clock signal

The DC-DC controller is synchronized by an internal clock signal (“CK”). The clock signal is internally generated by a “555 timer” block in astable configuration as per Figure 35.

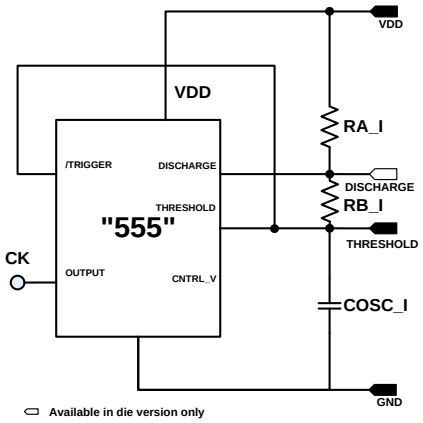


Figure 35: Internal oscillator scheme (for die version)

By default (when DISCHARGE and THRESHOLD are left floating), the internal oscillator generates a typical 180kHz clock signal at 25°C with a 90% duty cycle; this is based on following values for internal passive components:

RA_I	between VDD and DISCHARGE	36.4 KΩ
RB_I	between DISCHARGE and THRESHOLD	4.55KΩ
COSC_I	between THRESHOLD and GND	145 pF

The duty-cycle of the internal oscillator fixes the maximum duty-cycle of the DC-DC PWM control signal. The oscillator positive edge induces the positive edge of DC-DC PWMOUT output after some delay.

Both clock frequency and duty cycle can be adjusted by connecting external components to the THRESHOLD pin and/or the DISCHARGE pad (in die version).

For the packaged part (where only THRESHOLD pin is available), RC_E and COSC_E external components can be added as per Figure 36.

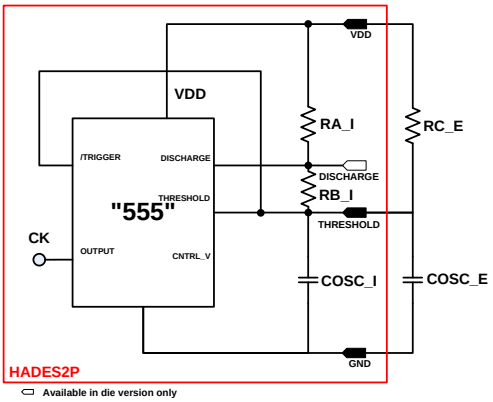


Figure 36: Oscillator with external components (for packaged version)

Frequency can lowered by adding COSC_E capacitor.

Frequency can increased up to 2 times the default value by adding RC_E component; frequency increase leads as well to maximum duty cycle change; Table 6 provides guidance on effect of RC_E/COSC_R values:

COSC_E value	RC_E value	Freq. (kHz)	Duty cycle
435 pF	∞	50	90%
145 pF	∞	95	90%
72 pF	∞	125	90%
0	∞	180	90%
0	150k	230	87%
0	75k	270	85%
0	30k	375	75%

Table 6: frequency/duty cycle change in function of RC_E

For the die version (where both THRESHOLD and DISCHARGE pads are available), RA_E/RB_E/COSC_E external components can be added as per Figure 37.

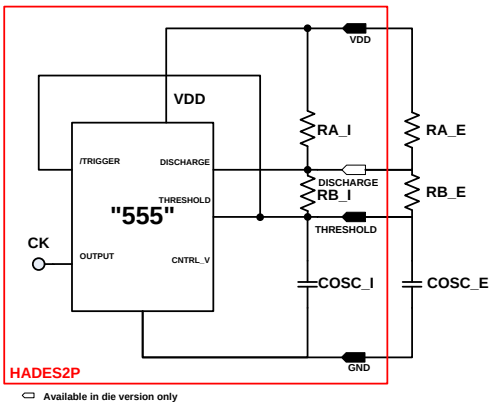


Figure 37: Oscillator with external components (die version)

Frequency and duty cycle can then be computed as follows:

- Fclk= 1.44/[(Ra + 2 Rb)*C]
- DC (%) = 100*(Ra+Rb)/(Ra+2*Rb)
- where:
  - Ra = RA_I // RA_E
  - Rb = RB_I // RB_E
  - C = COSC_I + COSC_E

The recommended usable frequency range is between 50kHz and 400kHz.

Soft-start

An internal soft-start function is implemented (no external components required); its time constant value is about 2 msec. This function is activated at each start-up and each time HADES2P is coming out of an internal fault state.

Error amplifier

It compares a fraction of the DC-DC converter output to the internal 2.5V reference. Its output V_{comp} is further compared by the internal comparator to a sawtooth in order to create a PWM signal.
To get an image of the DC-DC converter output, an auxiliary winding generating 5V is used. The output of this winding (AUX pin) is internally rectified by a diode and the resulting voltage (AUX_REC signal) is used as input to the voltage control loop.

Compensation network

HADES2P implementation of the control loop hardware supports all types of classical compensation networks (type I, II, III). In the die version (as shown on Figure 39), full flexibility is offered to the designer, while in the packaged part version (as shown in Figure 38), a 100K resistor is always present between FB_INT and FB pins.

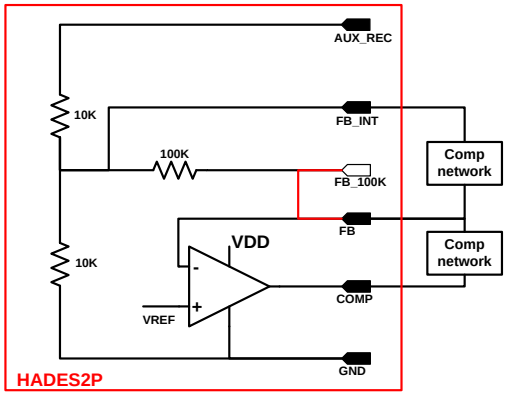


Figure 38: Compensation network implementation (packaged part)

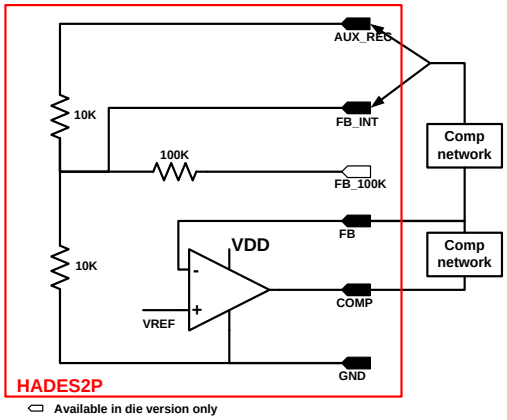


Figure 39: Compensation network implementation (die version)

Sawtooth, current sense/feedback & slope compensation

HADES2P implements a voltage and a current control loop.

The internal sawtooth signal (which is compared with error signal [COMP]) is generated internally as the sum of:

- an image of the THRESHOLD signal (with a typical gain of 0.3)
- an image of the switching current provided by the voltage on the PGND pin

To limit the effect of DC-DC power transistor switching noise on the sawtooth signal generation and to prevent false current limit detection, a 500 ns typ blanking time triggered by the turn on of the power transistor is implemented on the current sensing circuitry. During this time current sensing is not taken into account.

This internal sawtooth signal is available for debug purpose on SWT pin; however, this pin should be left unconnected at PCB level to minimize parasitic capacitance on SWT node.

This function behaves properly with Rshunt (cfr Figure 43) value as specified in the Electrical Characteristics section. Current loop gain (G_{CL}) depends on Rshunt value as per formula below:

- G_{CL} = 2.5*Rshunt (Volt/Ampere)

Rshunt value can be adapted by system designers if they pay attention to the impact of this change on the current loop gain and its potential effect of control loop stability.

Current limit

HADES2P performs a cycle-by-cycle current limiter. If during the time PWM is ON, the current through the switching transistor exceeds the limit, the cycle is aborted and PWM signal is brought back to OFF state.

The current limit threshold depends on the Rshunt (cfr Figure 43) value as per formula below:

- Actual current limit = Spec current limit * 0.5/Rshunt

So by adapting Rshunt value, current limit threshold can be modified.

It should be noted that there is a implementation related delay between the turn-on of the power transistor and the decision to turn if off because of to high current. Figure 27 provides guidance on this overload pulse duration.

Power switching and driver

HADES2P embeds an internal 80V 0.8Ω switching transistor suitable for most applications. However, to offer a scalable solution, the internal switching transistor driver output (PWMOUT) is also available enabling the use of an external transistor (in parallel with the internal transistor or independently); if internal switching transistor is not used, DRAIN signal must be connected to PGND.

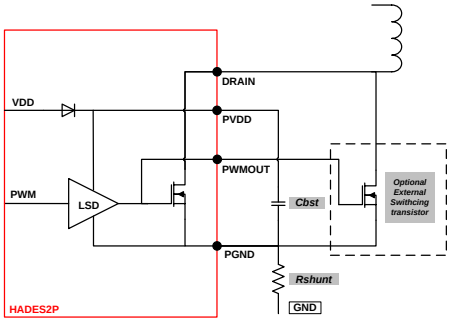


Figure 40. DC-DC output stage

In order to offer best performance in terms of Rdson and to enable use the switching transistor source terminal as current sense input, the power transistor is driven by a floating bootstrapped internal driver.
For proper operation of the internal driver, an external bootstrap capacitor is required between PVDD and PGND pins; this capacitor acts as power supply of the internal driver when the power transistor is ON.

Thanks to the very low current consumption of the internal driver and related level shifter and considering the DC-DC frequency range, the bootstrap capacitor dimensioning needs to obey to following rule:

$$33\text{nF} < C_{BST}(\text{nF}) < 200\ \text{nF}$$

Device power supplies and de-coupling scheme

Figure 41 illustrates the power supplies configuration and decoupling scheme.

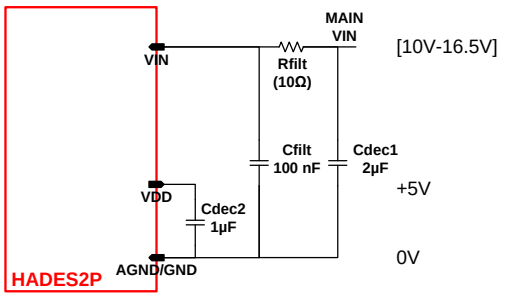


Figure 41. Power supplies configuration and decoupling

Rfilt and Cfilt implement a mandatory filter damping the voltage spikes generated by the high speed current variations on VIN. This filter should have a cut-off frequency set between 1 and 2 MHz; Rfilt dimensioning needs to take into account as well the average current flowing through this path. Typical values are: Rfilt = 10Ω, CF1 = 100 nF.
Cdec1 capacitor value has a typical value of 2µF; however, this value might need to be tuned in function of the gate driver function impedance requirements towards the upward systems (e.g. controller board).

Current consumption

HADES2P current consumption depends:

- On the state of both TX paths
- On the state of both RX paths
- # of used TX channels
- On the state of the DC-DC converter

Table below provide guidance on the current consumption of the HADES2P device (VIN=15V).

STATE	I_{VIN} [mA]
Primary and secondary's in fault	2.55
Primary OK and secondary's in fault; DINx=0	4.4
Primary and secondary's OK; DINx=0	7.4
Primary and secondary's OK; DINx=20kHz 50% DC on each PWM signal	7.4+ (DCA+DCB)*9.3

where:

- DCA: duty cycle of channel A (0: unused, 1: 100% duty cycle)
- DCB: duty cycle of channel B (0: unused, 1: 100% duty cycle)

It should be noted that in fault state, DOUT pins draw current; however, this current comes from external VIN and not from the HADES2P VIN pin and so is not included in the formula.
The DC-DC switched current (flowing between DRAIN and PGND pins) is also not included in those calculations.

Power dissipation

Power dissipation inside HADES2P device is coming from 3 sources:

- the current through VIN pin; typical power dissipation in normal operation and with VIN = 15V is 250 mW
- the resistive losses of the DC-DC internal switching transistor; this depends of course heavily on the average current supplied by the DC-DC converter to the secondaries
- the switching losses of the DC-DC internal switching transistor; this can be estimated to about 70 mW which can be considered as negligible with respect to the 2 other sources of dissipation.

The following graph provides information on total device power dissipation (normal operation) in function of PWM switching frequency (DC=50%) and of secondary power device gate charge; the maximum Y-axis value corresponds to the maximum power dissipation supported by CHT-HADES2P packaged part.

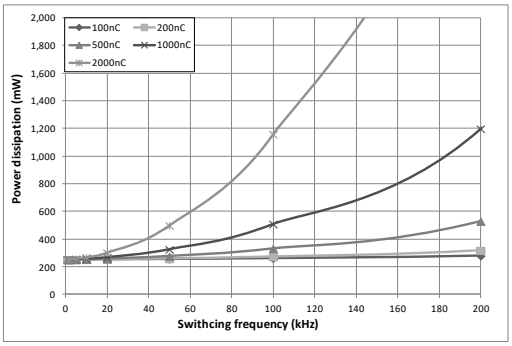


Figure 42. Power dissipation in CHT-HADES2P

Application Diagram

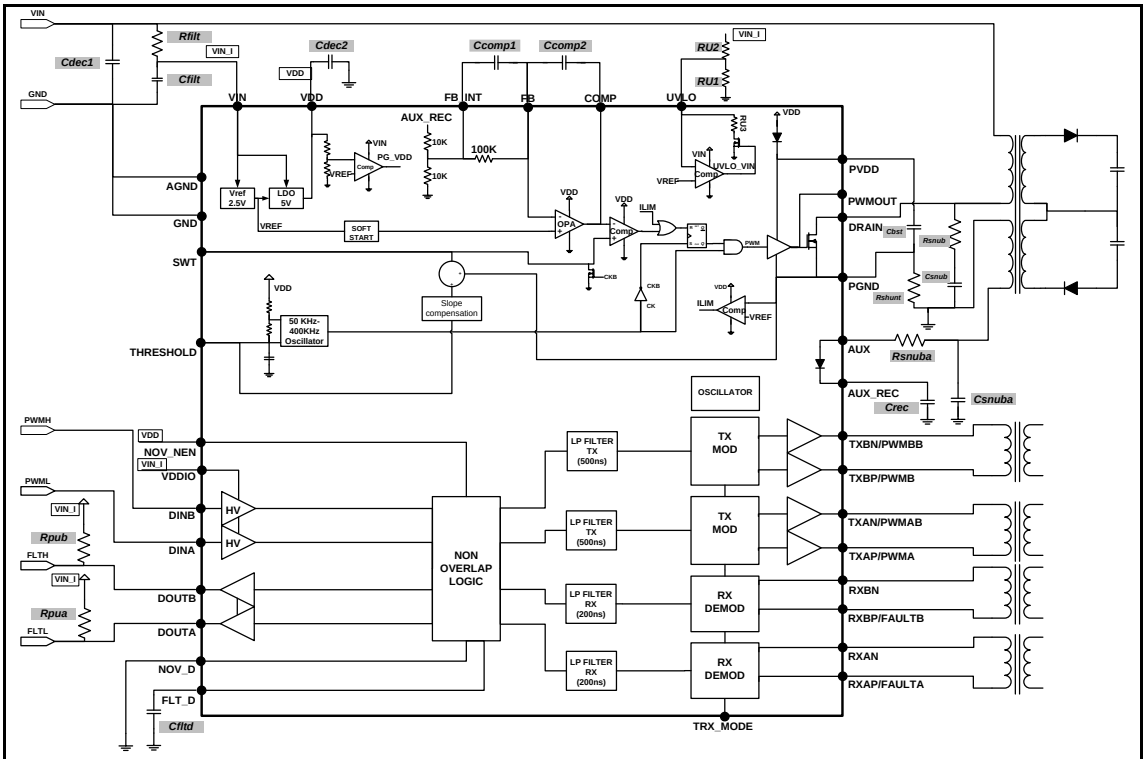


Figure 43: Application diagram

This application diagram reflects an implementation where:

- PWM input signals have a voltage swing equal to VIN
- Fault DOUT signals have a voltage swing equal to VIN
- the PWM channels are independent of each other
- input spike filter on PWM signals is not active

The application schematic shows the implementation of Type II transfer function compensation scheme implementing a zero and a pole

$$f_z = \frac{1}{2\pi C_1 R_1}$$

$$f_p = \frac{21}{2\pi * C_1 R_1} = 21 f_z$$

Where R1 equals 100K (internal resistor) while Ccomp1 is to equal to C1.

The size of the capacitor has to be sized appropriately together with it's parallel discharging resistance (present in the form of FB resistive divider on the application schematic) with respect to switching frequency (reasonable voltage ripple on AUX_REC signal) and should be close the R/C constant expected on the output of the fly-back (represented by output filtering capacitors and the expected load change on the output).

If the application only requires 1 channel (PWM/FLT), channel B should be used and following change should be applied to this application diagram:

- leave DOUTA open
- connect RXAN/RXAP to GND
- connect DINA to GND

Application diagram (cnt'd)

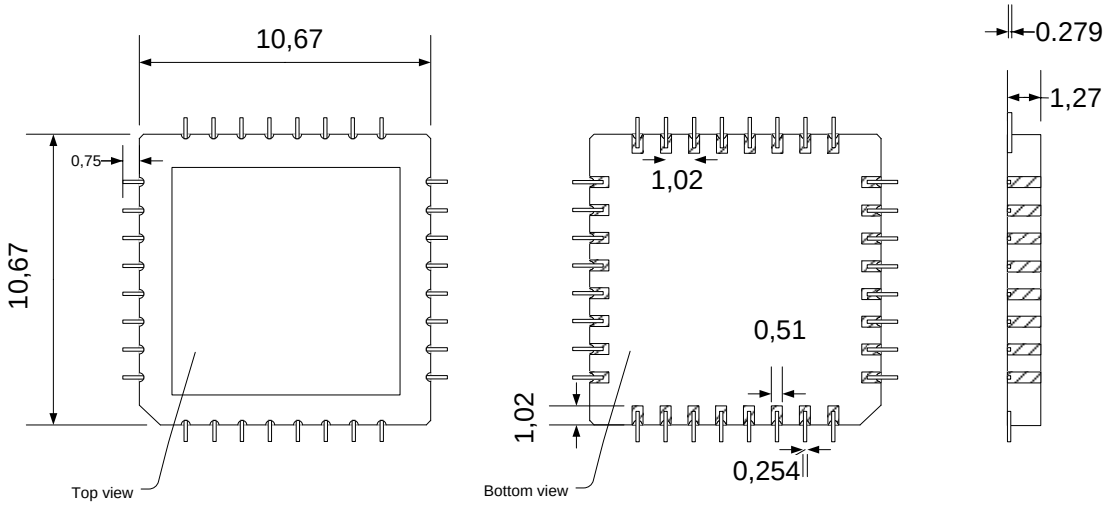
Table below lists all required passive devices in the typical application drawn in Figure 43 and provides guidance on typical value and important selection criteria for those passives.

Passive ID	Type	Function	Typ. Value (Capacitor dielectric)	Typ. Operating Voltage/ Power	Rated Voltage/ Power	Comment
Cdec1	C	Main decoupling capacitor on VIN	2µF (X7R)[8]	20V	50V	
Rfilt	R	Spike filtering	[1-20]Ω	10mW	TBD[9]	
Cfilt	C	Decoupling and filter capacitor	100 nF (X7R)8	20V	50V	
Cdec3	C	Voltage regulator output capacitor	1µF (X7R)8	5V	10V	ESR typ. : 100mΩ
RU1	R	UVLO threshold setting				Refer to section Under-Voltage Lockout (UVLO) [page 15] for dimensioning information
RU2	R	UVLO threshold setting				Refer to section Under-Voltage Lockout (UVLO) [page 15] for dimensioning information
Rpua	R	Pull-up resistor	> 300Ω			Pay attention to power dissipation when selecting component
Rpub	R	Pull-up resistor	> 300Ω			Pay attention to power dissipation when selecting component
Cfltd	C	Fault timer value setting	Depends on system design	5V	10V	Refer to section PWM&FAULT datapath for dimensioning information
Cbsth	C	Bootstrap capacitor	[33-200]nF8	5V	10V	
Rshunt	R	Shunt resistor	0.5Ω			
Crec	C	Rectification capacitor		5V	10V	Cfr description above
Rsnub	R	Primary winding snubber resistor				Value depends on transformer characteristics
Csnub	C	Primary winding snubber capacitor		50V	100V	Value depends on transformer characteristics
Rsnuba	R	Auxiliary winding filter resistor				Value depends on transformer characteristics
Csnuba	C	Auxiliary winding filter capacitor		30V	50V	Value depends on transformer characteristics
Ccomp1	C	Control loop filter		5V	10V	Value depends on filter characteristics
Ccomp2	C	Control loop filter		5V	10V	Value depends on filter characteristics

[8] Value at room temperature, considering a voltage and temperature derating of -66% at the operating voltage and 225°C

[9] Depends on resistor max rated operating temperature and application max ambient temperature

Package Drawing



CQFP32 physical dimensions in mm (tolerance : +/- 0.2 mm)

Ordering Information

Product Name	Ordering Reference	Package	Marking
CHT-HADES2P	CHT-TIT9687B-CQFP32-T	CQFP32	CHT-TIT9687B

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 11 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 – F : +32 10 88 98 75 Email : sales@cissoid.com
Sales Representatives:	**Visit our website: http://www.cissoid.com**

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