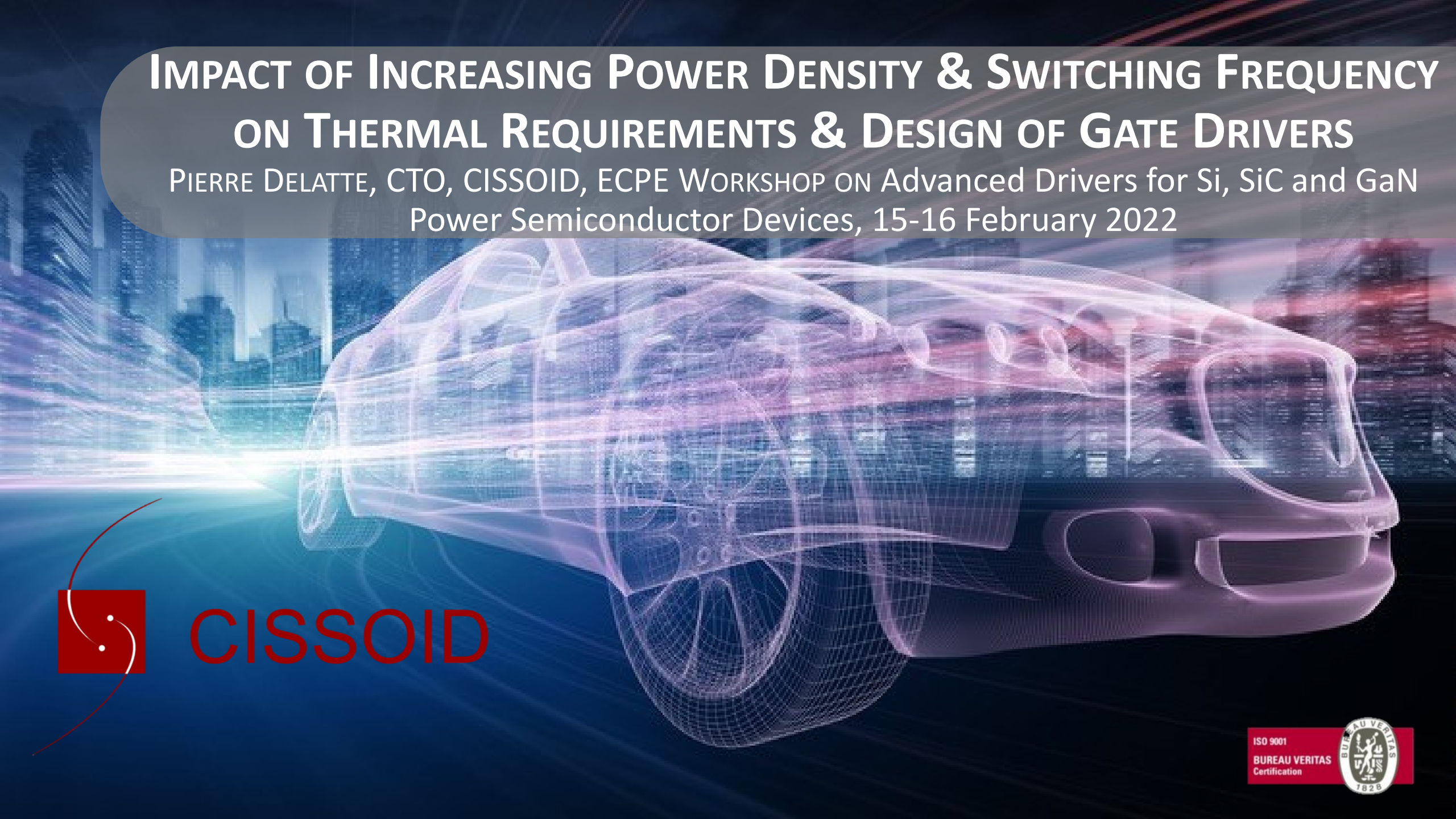
Impact of Increasing Power Density & Switching Frequency on Thermal Requirements & Design of Gate Drivers

Pierre Delatte, CTO, CISSOID, ECPE Workshop on Advanced Drivers for Si, SiC and GaN Power Semiconductor Devices, 15-16 February 2022



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AGENDA

- Introduction
- Gate drivers for Wide Bandgap devices
- Gate driver thermal design
- Gate driver/power module co-design
- Conclusion

OBJECTIVES

- To give an insight into the impact of higher power density on gate driver thermal design
- To focus on gate drivers for high voltage/high current SiC power modules

12 Years of Innovation in SiC Gate Drivers & Power Modules at CISSOID

SiC-based Solutions for efficient power conversion and compact motor drives

2011 — 1st SiC Gate Driver ICs
High Temperature Gate Driver Chipset

2013 — 225°C discrete SiC MOSFET
10A/1200V SiC MOSFET in TO-257

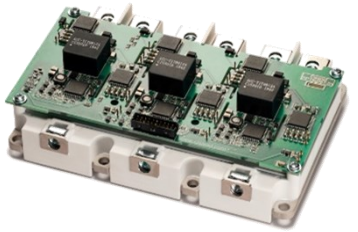
2015 — 225°C SiC MOSFET Module
Dual 30A/1200V SiC MOSFET

2015 — 2nd Gen SiC Gate Driver ICs
2nd Generation Gate Driver Chipset

2016 — 1st SiC MOSFET IPM
3-Phase 1200V/200A SiC IPM for Aerospace

2019 — 125°C SiC Gate Driver Board
For 62mm & XM3 SiC MOSFET Power Modules

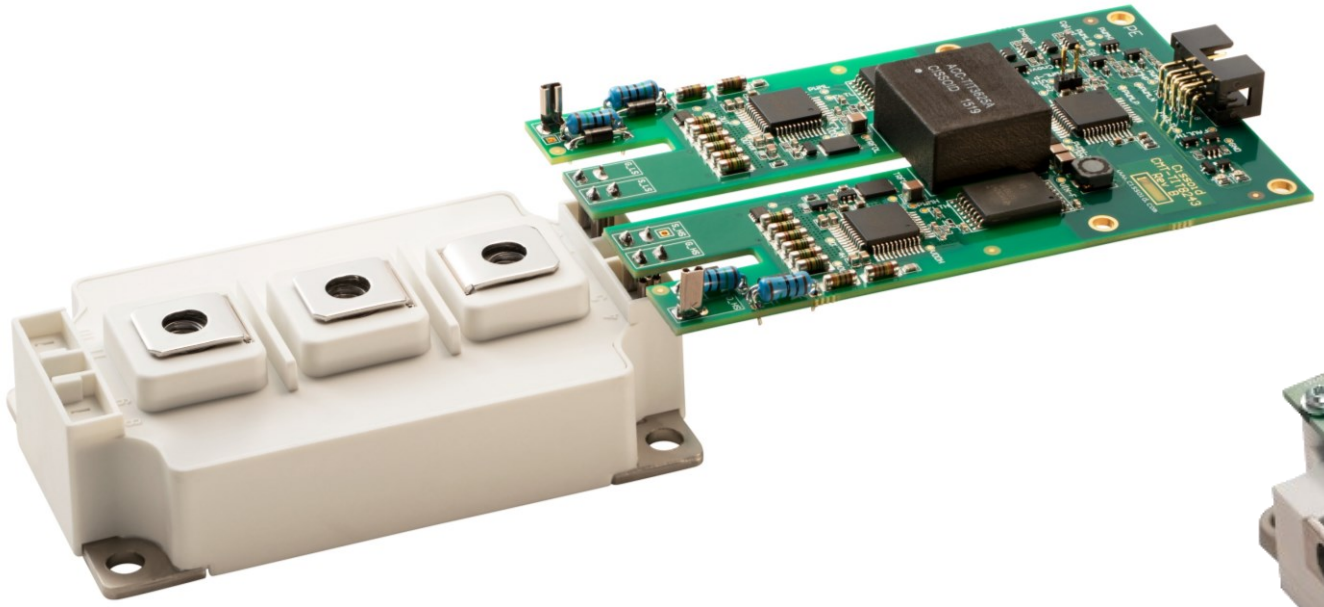
2020 — SiC MOSFET IPM For E-Mobility
3-Phase 1200V/450A SiC IPM for E-Mobility



SiC Gate Drivers

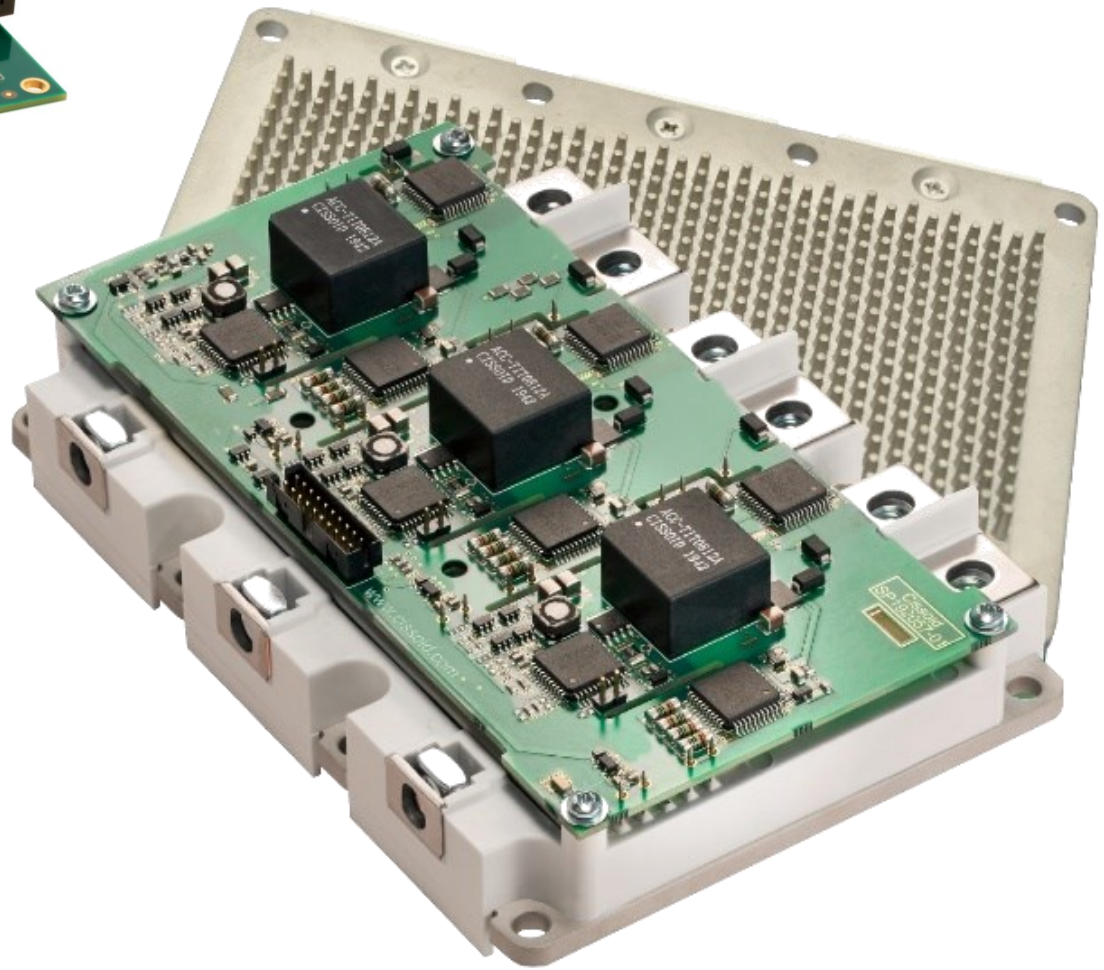
Reliable SiC Power Packaging

SiC Intelligent Power Modules (IPM)



125 ℃ Gate Driver Board
for 1200V-1700V 300A-450A
SiC 62mm Power Modules

GATE DRIVERS FOR WBG



3-Phase 1200V/340A-550A
SiC MOSFET Intelligent Power
Module (IPM) with AlSiC pin fin
Baseplate for liquid cooling

TRENDS WITH WBG POWER TRANSISTORS

WBG Power devices enable higher power density thanks to

- **Faster switching, higher dV/dt & dI/dt**

  → lower switching losses

- **Higher switching frequencies**

  → Smaller filters/magnetics

SiC & GaN

- **Higher operating voltages**

  → Reduced currents/conduction losses, e.g., with transition to 800V BEV

- **Higher junction temperatures**

  → Reduced cooling

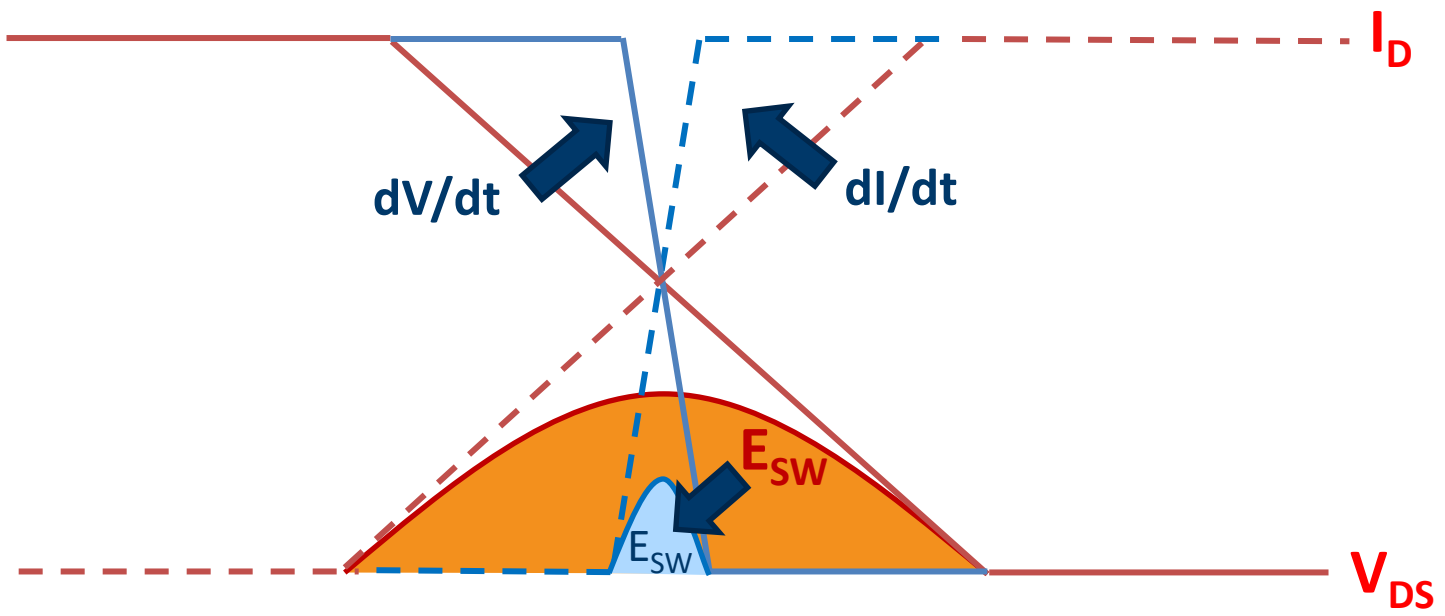
SiC

FASTER SWITCHING

Fast switching WBG transistors enable lower switching losses and higher switching frequencies

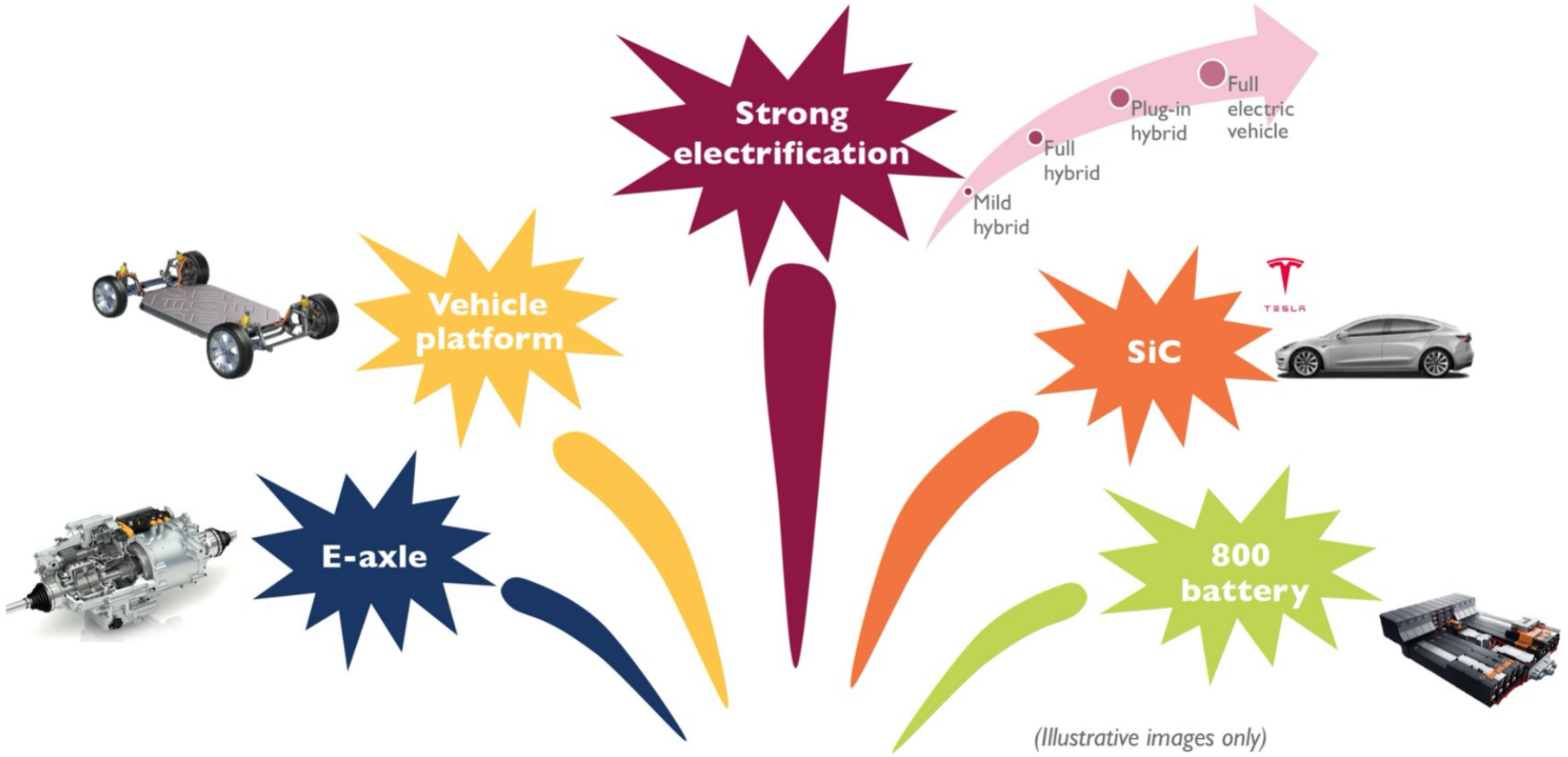
→ Higher efficiency

→ Smaller filters & magnetics



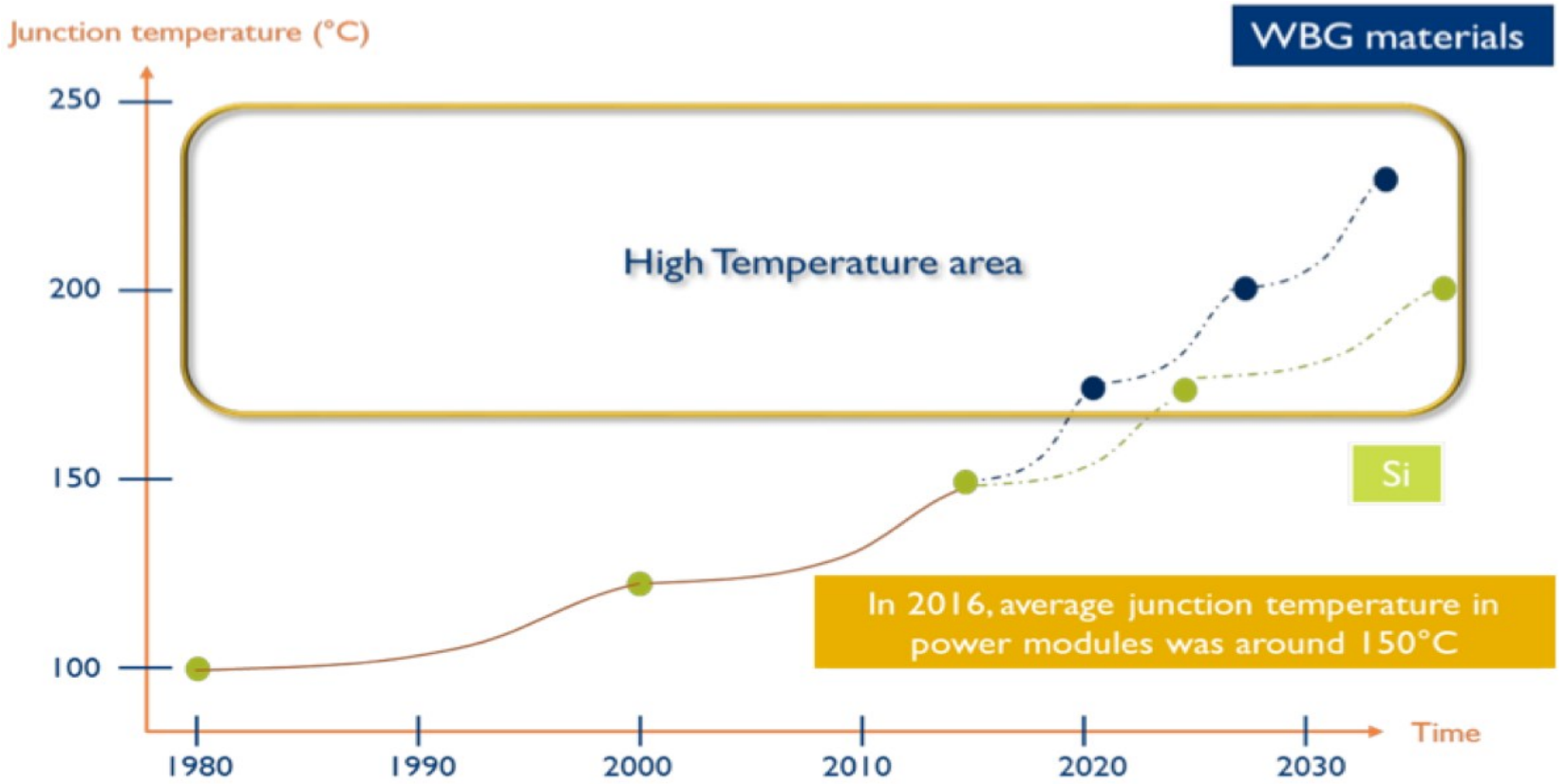
HIGHER OPERATING VOLTAGES WITH SiC

Transition to 800V BEV increases efficiency & reduces charging time



Higher Junction Temperature in Power Modules

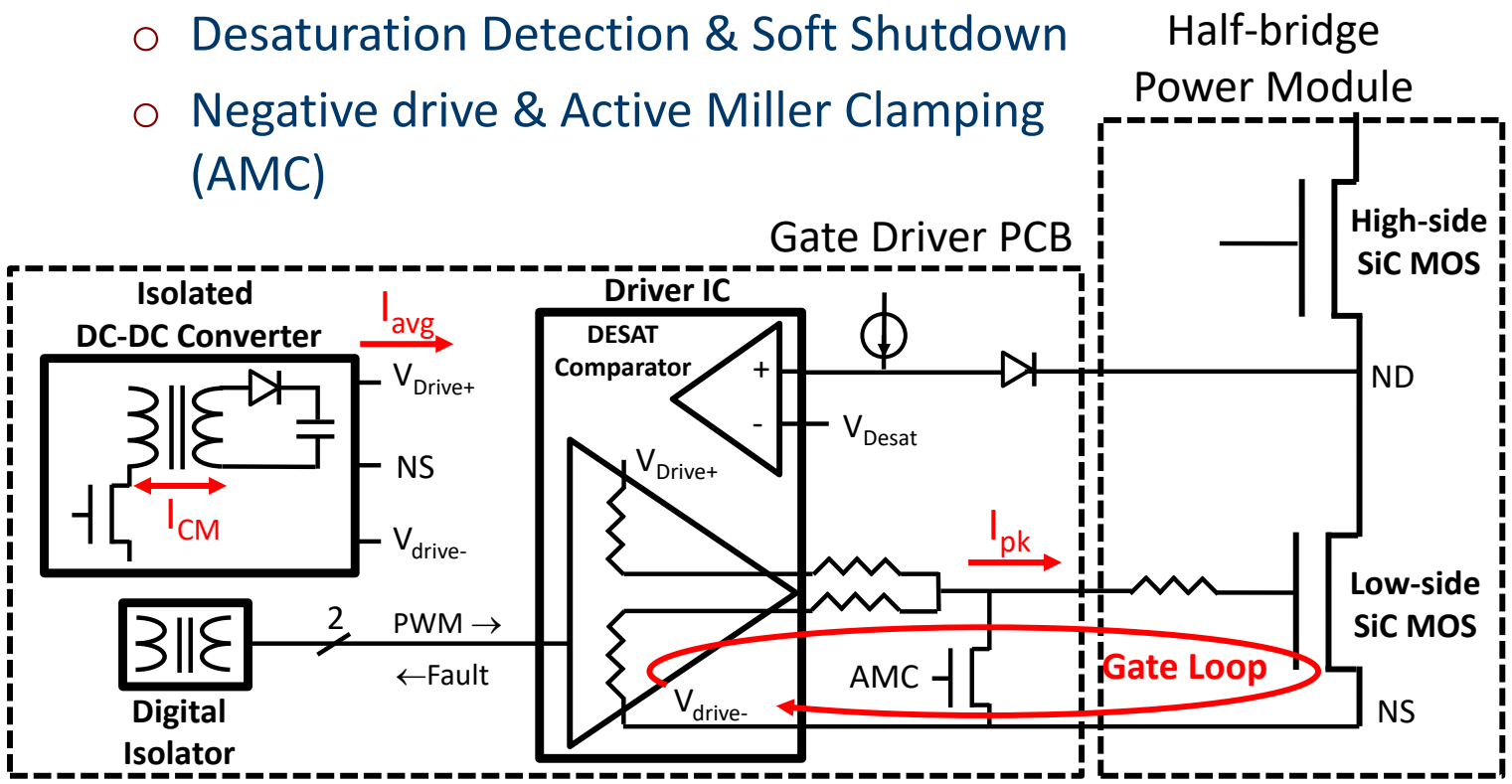
SiC Technology continues to push junction temperature higher

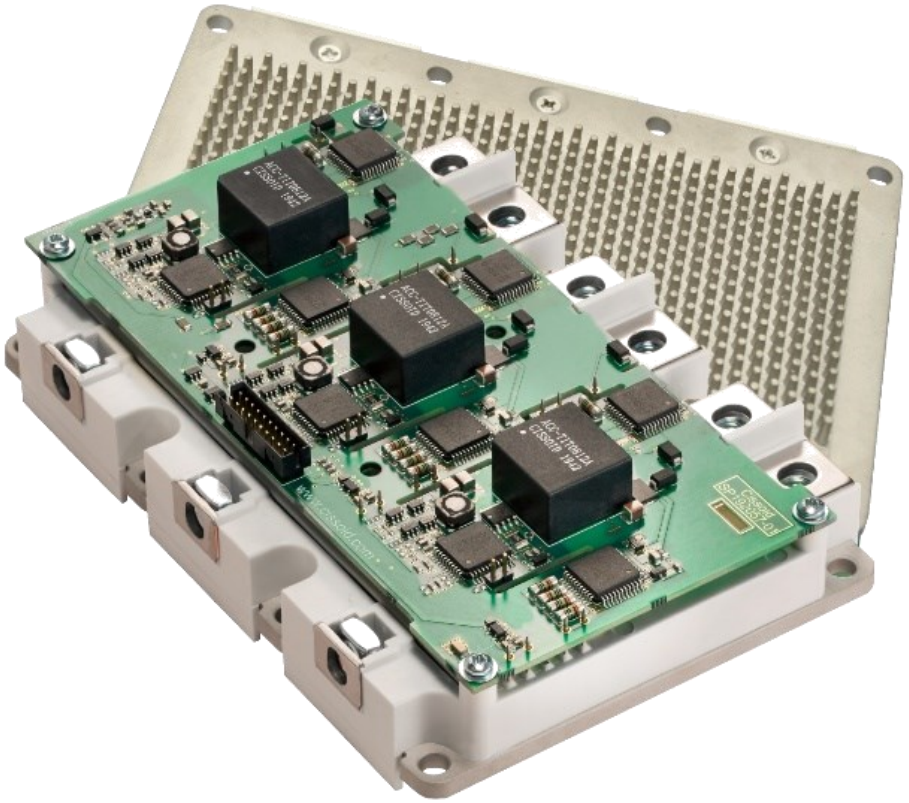


Source:

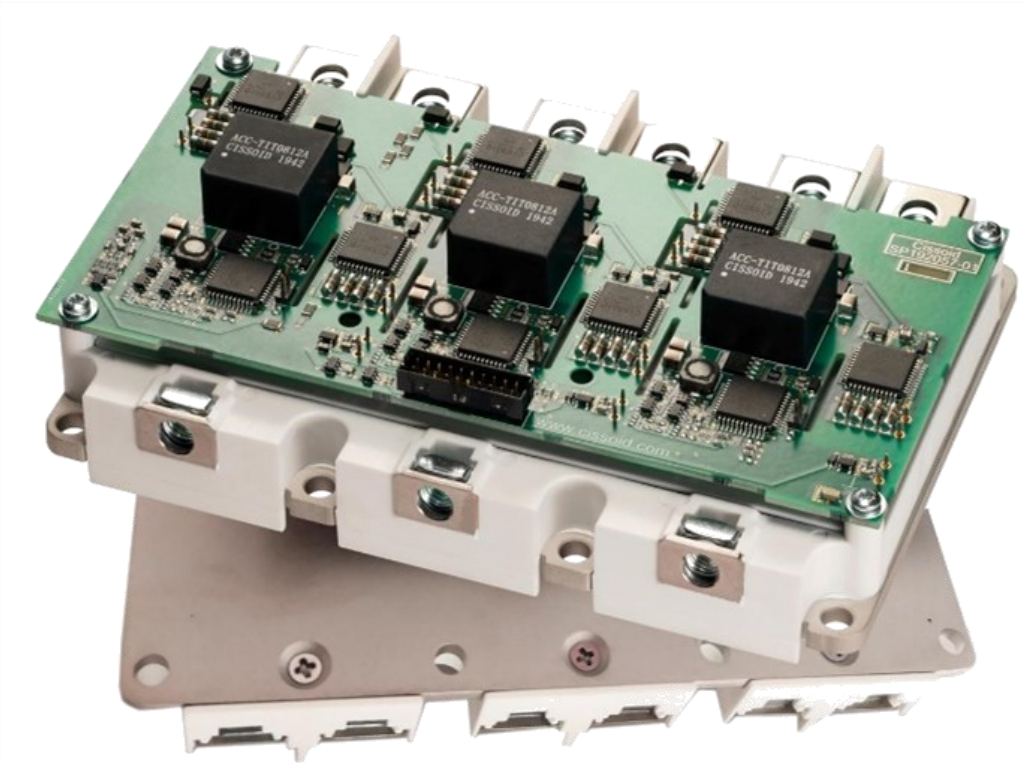
SiC/GaN Gate Driver Requirements

- Fast switching
  - Higher peak gate currents I_{pk}
  - High common-mode currents I_{CM}
  - Lower gate loop inductance
  - Integration with power module
- High switching frequencies
  - High average gate current I_{avg}
  - Power dissipation in gate loop
- High Voltage
  - Isolation/Creepage/Clearance
- High temperature
  - T_{amb}: 85°C … 125°C for high power density
- Accurate driving voltages (+/-5%)
  - For gate oxide long-term reliability
- Protection functions
  - Desaturation Detection & Soft Shutdown
  - Negative drive & Active Miller Clamping (AMC)





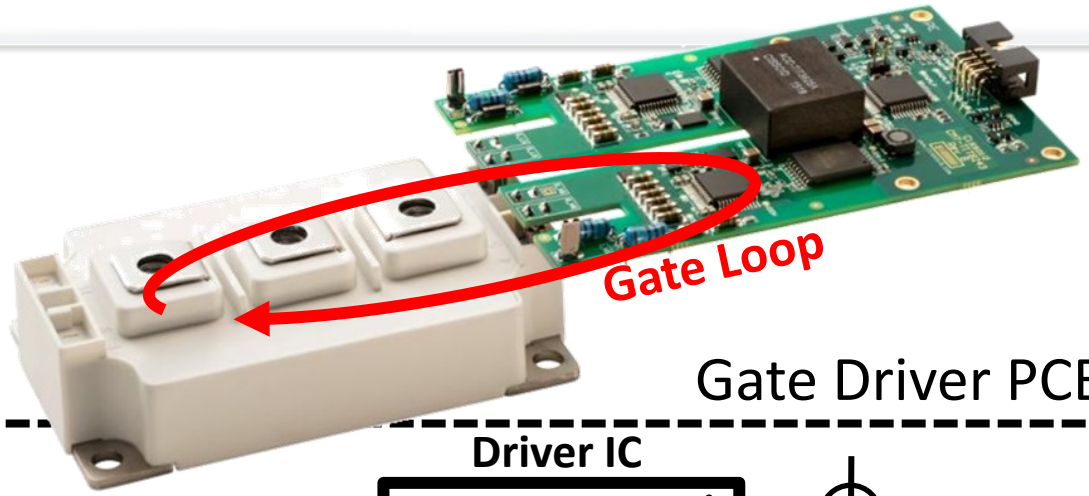
SiC IPM with AlSiC pin fin Baseplate for liquid cooling



SiC IPM with AlSiC flat Baseplate

GATE DRIVER THERMAL DESIGN

Driver/Power Module Gate Loop



Half-bridge
Power Module

Gate Driver PCB

Isolated
DC-DC Converter

V_{Drive+}

NS

V_{drive-}

Digital
Isolator

2

PWM →

←Fault

Driver IC

DESAT
Comparator

+

-

V_{Desat}

V_{Drive+}

V_{drive-}

AMC

High-side
SiC MOS

ND

Low-side
SiC MOS

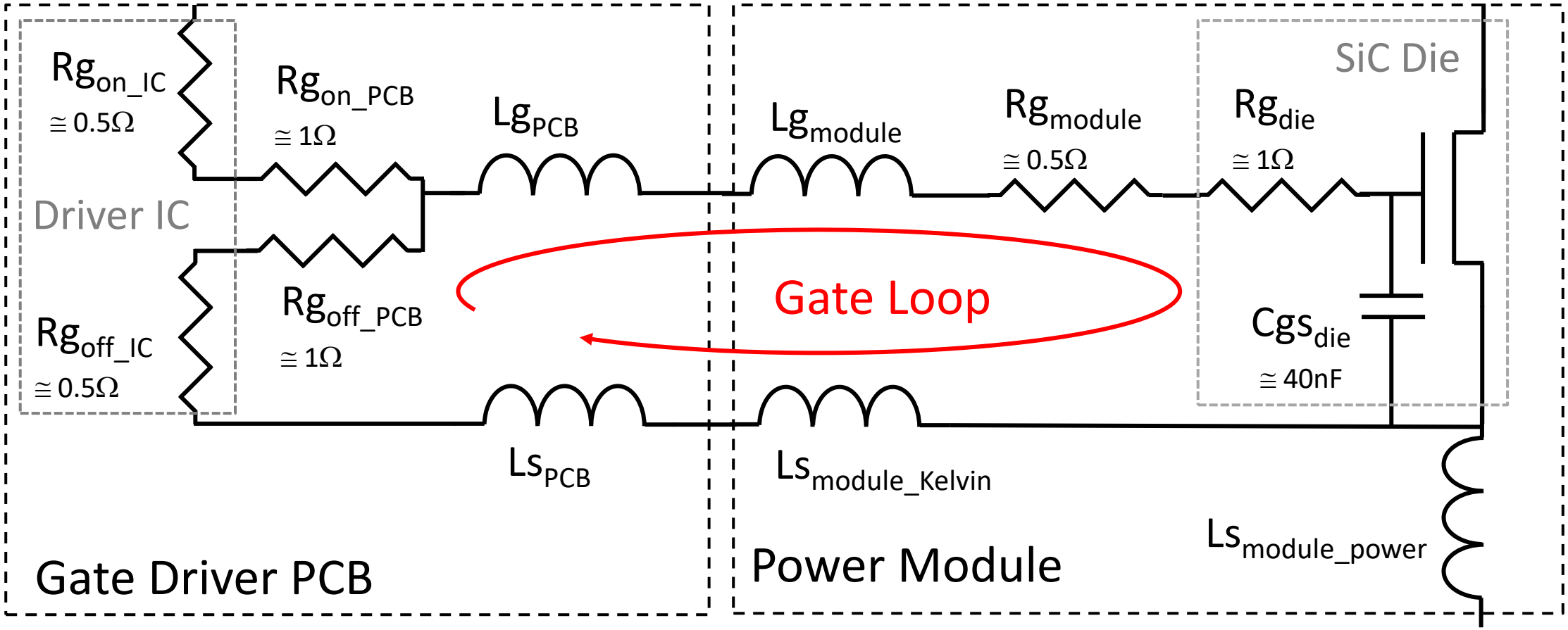
Gate Loop

NS

Driver/Power Module Gate Loop

With typical values for 1200V/450A-550A SiC MOSFET Module

- $R_{g\_tot} \cong 3\Omega$, C_{gs}=40nF $\rightarrow$ $L_{g\_tot} < C_{gs}*(R_{g\_tot}/2)^2$ = 90nH for no ringing



Gate Driver Power Requirements

With typical values for 1200V/450A-550A SiC MOSFET Module

- Gate charge: Q_{gate} = 910nC … 1500nC → consider **1125nC**
- Driving voltages: V_{drive}=+15V/-3V
- Gate resistor: 2Ω…4Ω for fast switching
  - Gate driver chip: 0.3Ω … 0.6Ω → ≅ **0.5Ω**
  - Gate driver PCB: 0.5Ω … 2.5Ω → ≅ **1Ω**

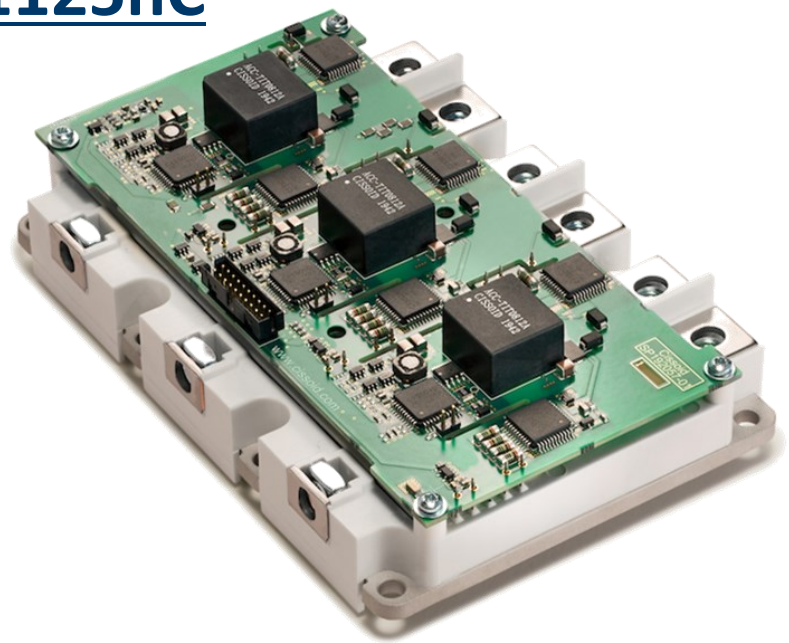
  } → 50%

  - Inside power module: 0.5Ω … 2.5 Ω → ≅ **1.5Ω** → 50%
- Power dissipation in gate loop
  - At 25kHz: $P_{gate}=Q_{gate}*V_{drive}*F$ ≅ 0.5W
  - At 100KHz: $P_{gate}=Q_{gate}*V_{drive}*F$ ≅ 2W

  } Power dissipation spreading is proportional to gate resistor distribution!

  → ≅ 50% or 1W in the power module

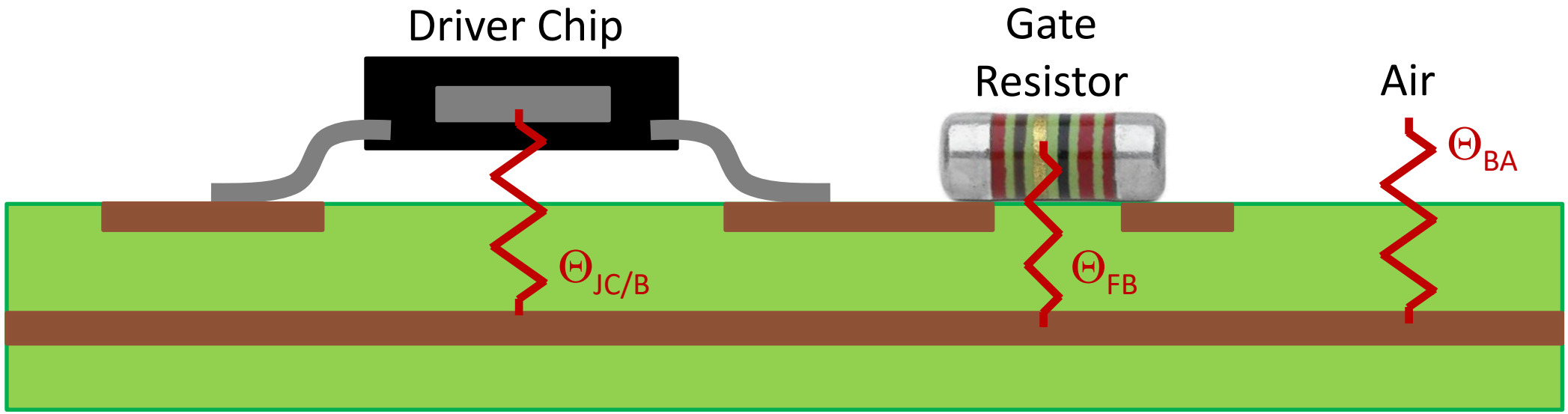
  → **≅ 50% or 1W/channel on the gate driver PCB!**



GATE DRIVER POWER REQUIREMENTS

PCB/DRIVER CHIP/GATE RESISTOR THERMAL MODEL

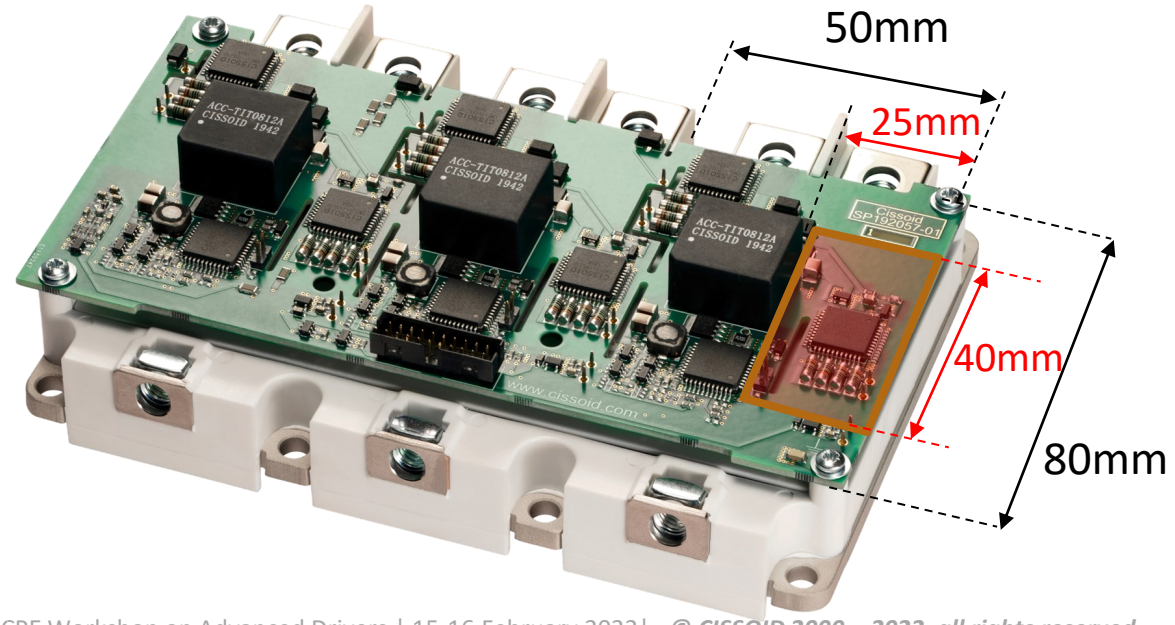
- Θ_{JB} is the junction-to-board thermal resistance (driver chip)
  - It is considered that $\Theta_{JC} \cong \Theta_{JB} (T_{Case(bottom)} \cong T_{Board})$ [Ref 1]
- Θ_{FB} is the film-to-board thermal resistance (gate resistor) [Ref 2]
- Θ_{BA} is the board-to-ambient thermal resistance (PCB)

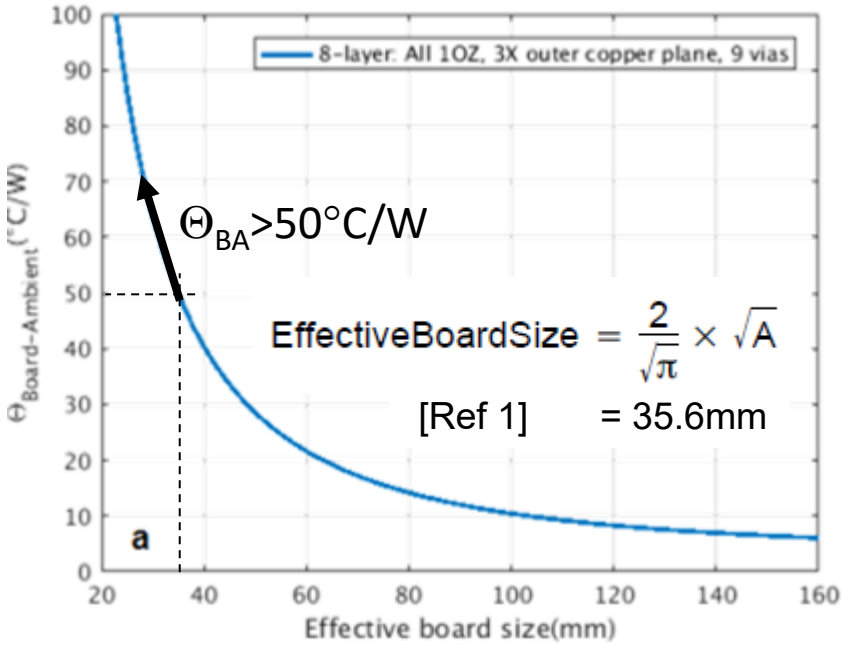


Gate Driver Power Requirements

Board-to-ambient thermal resistance

- PCB area per phase to fit on top of power module: 80mm*50mm
- In the best case, Area/4 per isolated driver channel : A=40mm*25mm=1000mm²
  - In practice, further constrained by isolation/creepage requirements
- Board-to-air thermal resistance $\Theta_{BA} > 50°C/W \rightarrow \Delta T_{BA} > 50°C$ at 1W@100kHz
  - At T_A=90°C -> T_{Board} > 140°C, approaching or exceeding the temperature limit of FR4 PCBs





GATE DRIVER POWER REQUIREMENTS

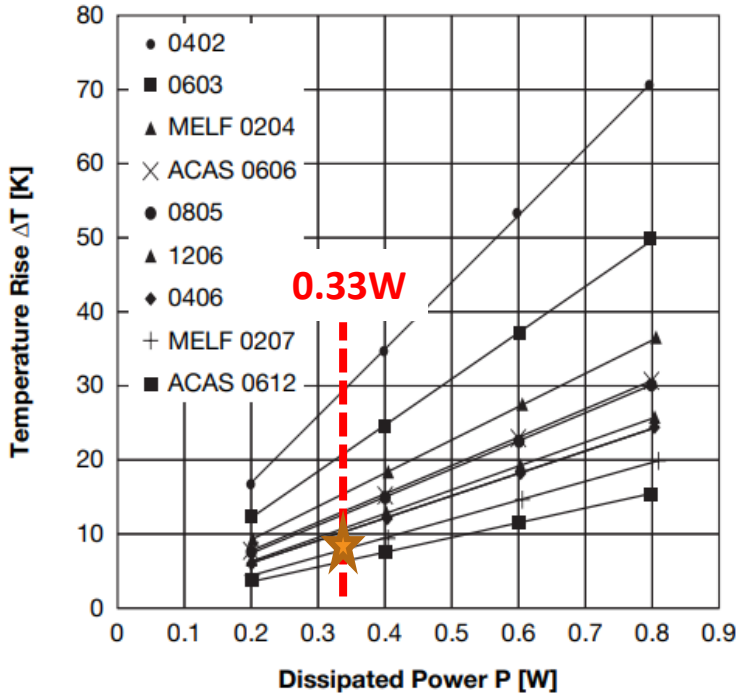
JUNCTION-TO-BOARD THERMAL RESISTANCE

- Junction-to-board thermal resistance Θ_{JB} is strongly dependent on the chip packaging technology
  - A few °C/W for a package with exposed thermal pad
  - About 35°C/W for a SOIC16 package commonly used for isolated gate driver ICs
- Based on previous hypotheses, about 1/6 of the power is dissipated in the gate driver chip, i.e. 0.33W for P_{gate}=2W
  - For Θ_{JB} = 35°C/W, ΔT_{JB} = 11.5°C
  - For $T_{Board} > 140°C \rightarrow T_J > 150°C$, exceeding T_{Jmax} of most driver ICs

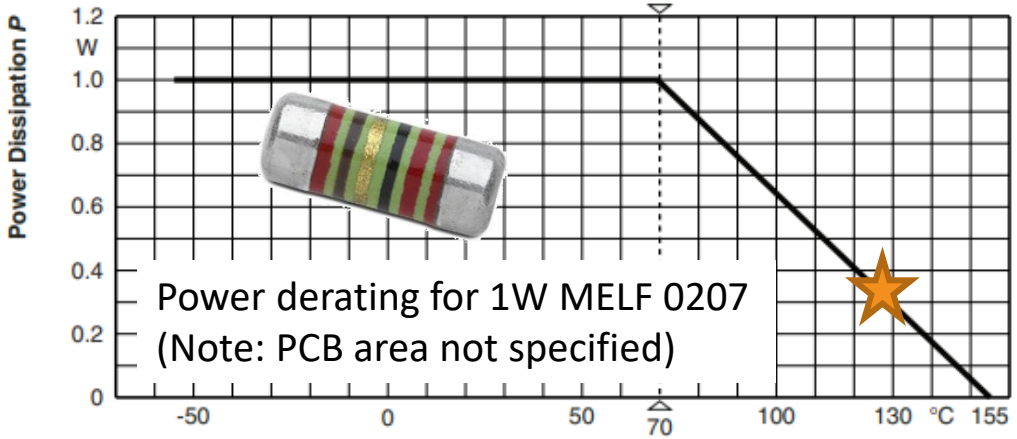
GATE DRIVER POWER REQUIREMENTS

FILM-TO-BOARD THERMAL RESISTANCE

- Based on previous hypotheses, about 1/3 of the power is dissipated in PCB gate resistors, i.e. 0.66W for P_{gate}=2W
  - → 0.33W per R_{on_PCB} / R_{off_PCB}
- High-power resistors are required
  - MELF 0207: Θ_{FB} =26°C/W [Ref 2]
  - ΔT_{FB}@0.33W = 8.5°C
- At T_{board} > 140°C → T_{film} > 148.5°C
  - Putting two MELF 0207 resistors in parallel is relaxing thermal constraints
  - Note that derating curve is too optimistic because it considers a larger PCB area

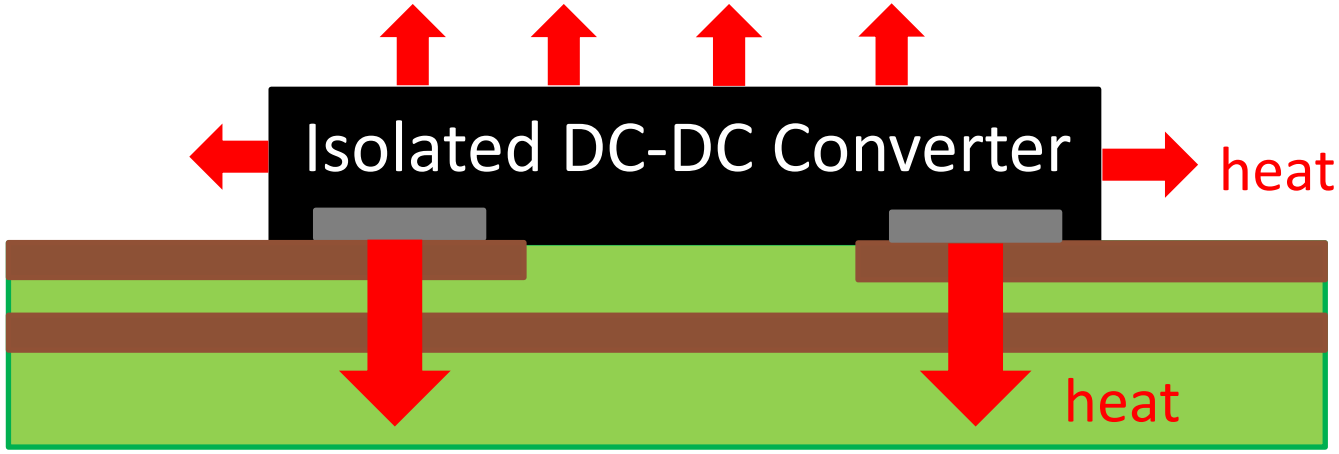


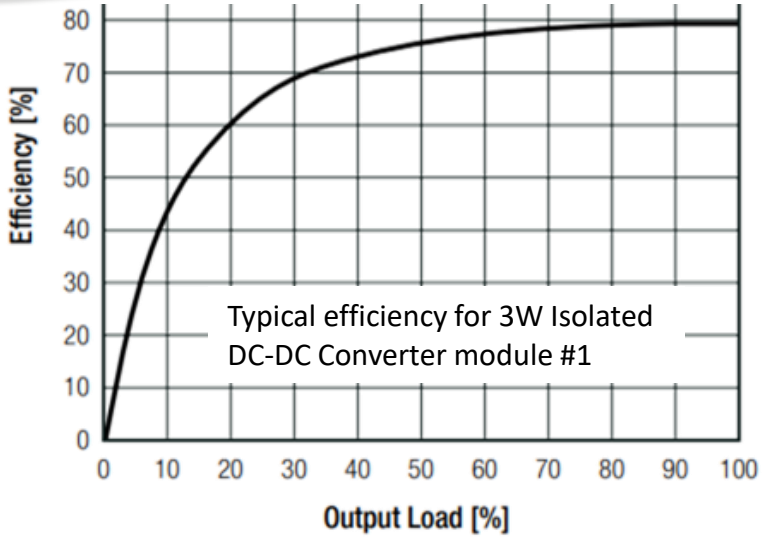
$\Delta T_{Film\text{-}to\text{-}case}$ for different types of resistors [Ref 2]

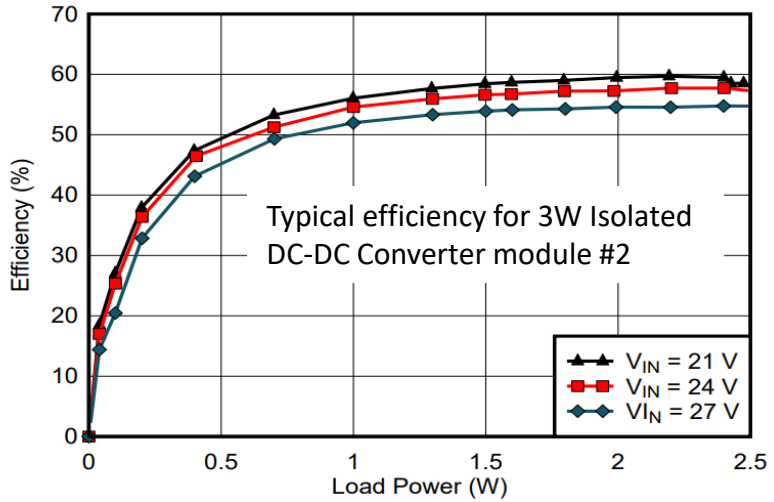


Power & Thermal Requirements for Gate Driver Isolated DC-DC Converter

- At V_{drive}=+15V/-3V & Qg=1125nC
  - 25kHz → 100KHz: Pout = 0.5W → 2W
- For 2W output power
  - Typ. Efficiency @25°C = 80% → Losses > 0.5W
  - Typ. Efficiency @25°C = 60% → Losses > 1.33W!
- Contributing to further PCB heating

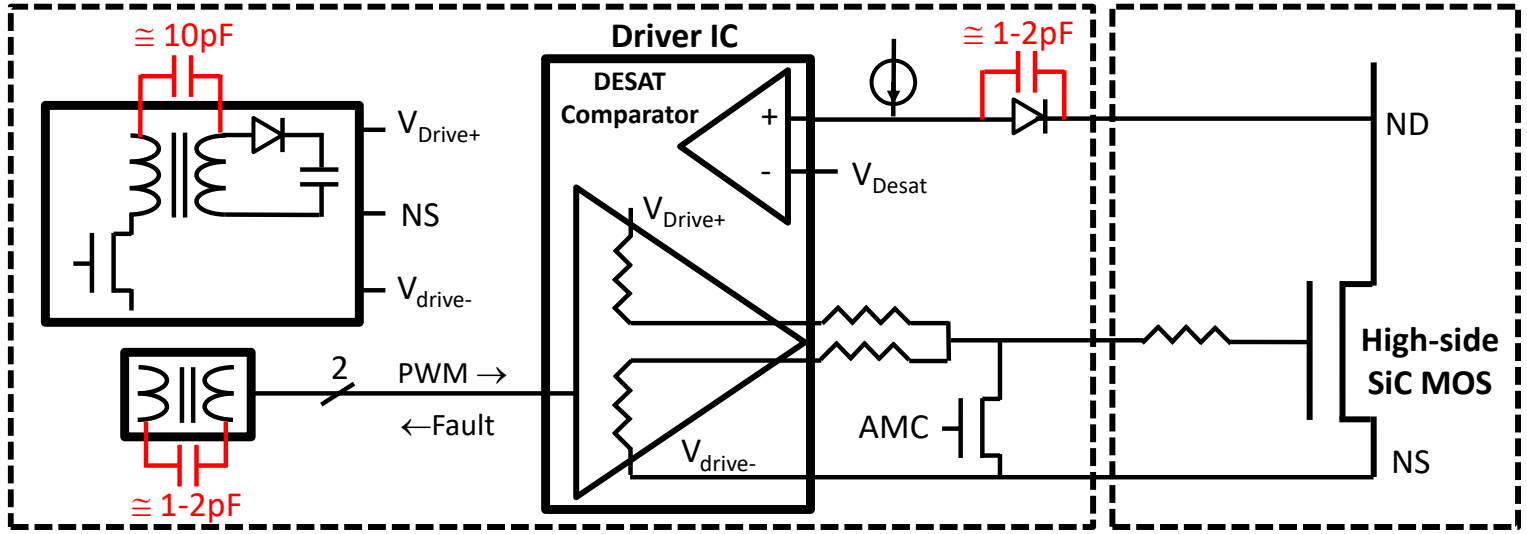


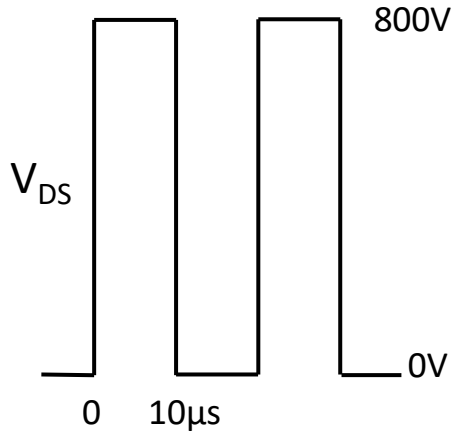




Power Dissipation in Gate Driver due to High Voltage & High Frequency Switching

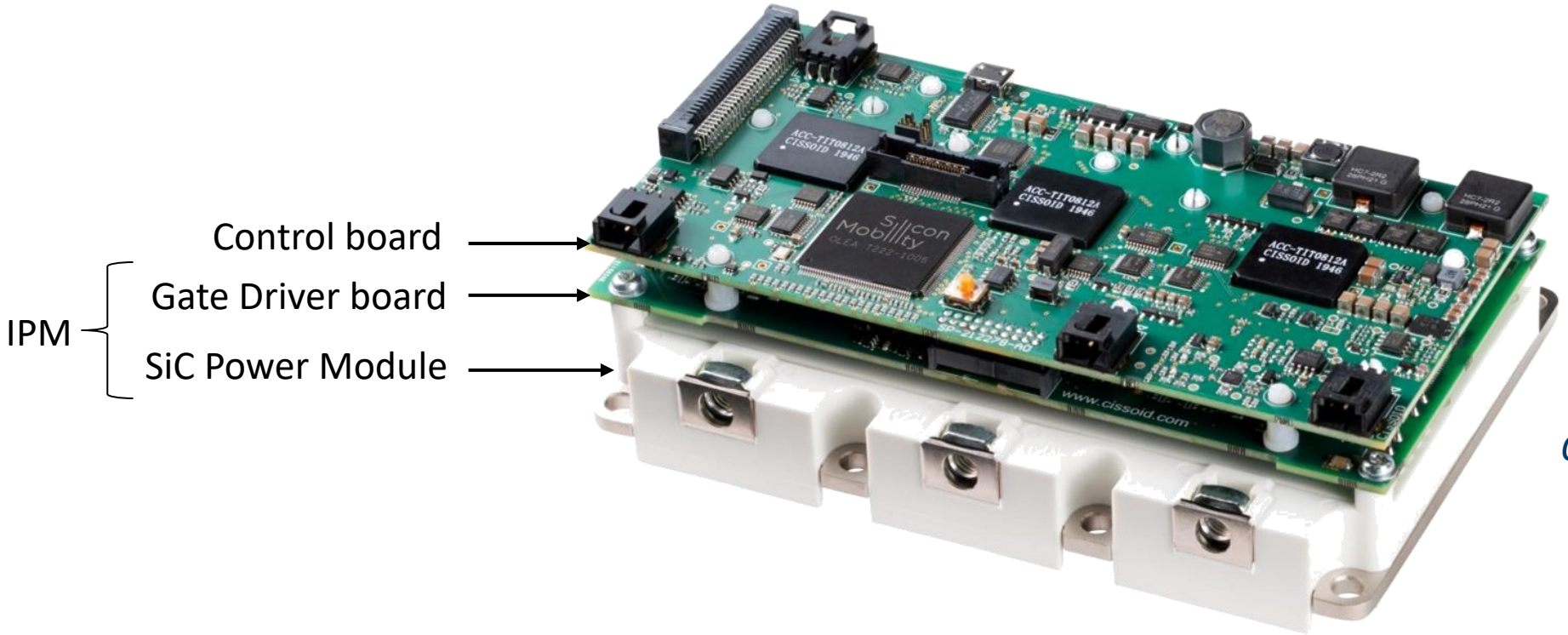
- As the power module is switching, some capacitors are charged and discharged at each cycle
- At 800V/100kHz: Losses=12pF*800V²*100kHz=768mW
- It is difficult to pinpoint where these losses are dissipated but it adds to the total power losses on the gate driver PCB!



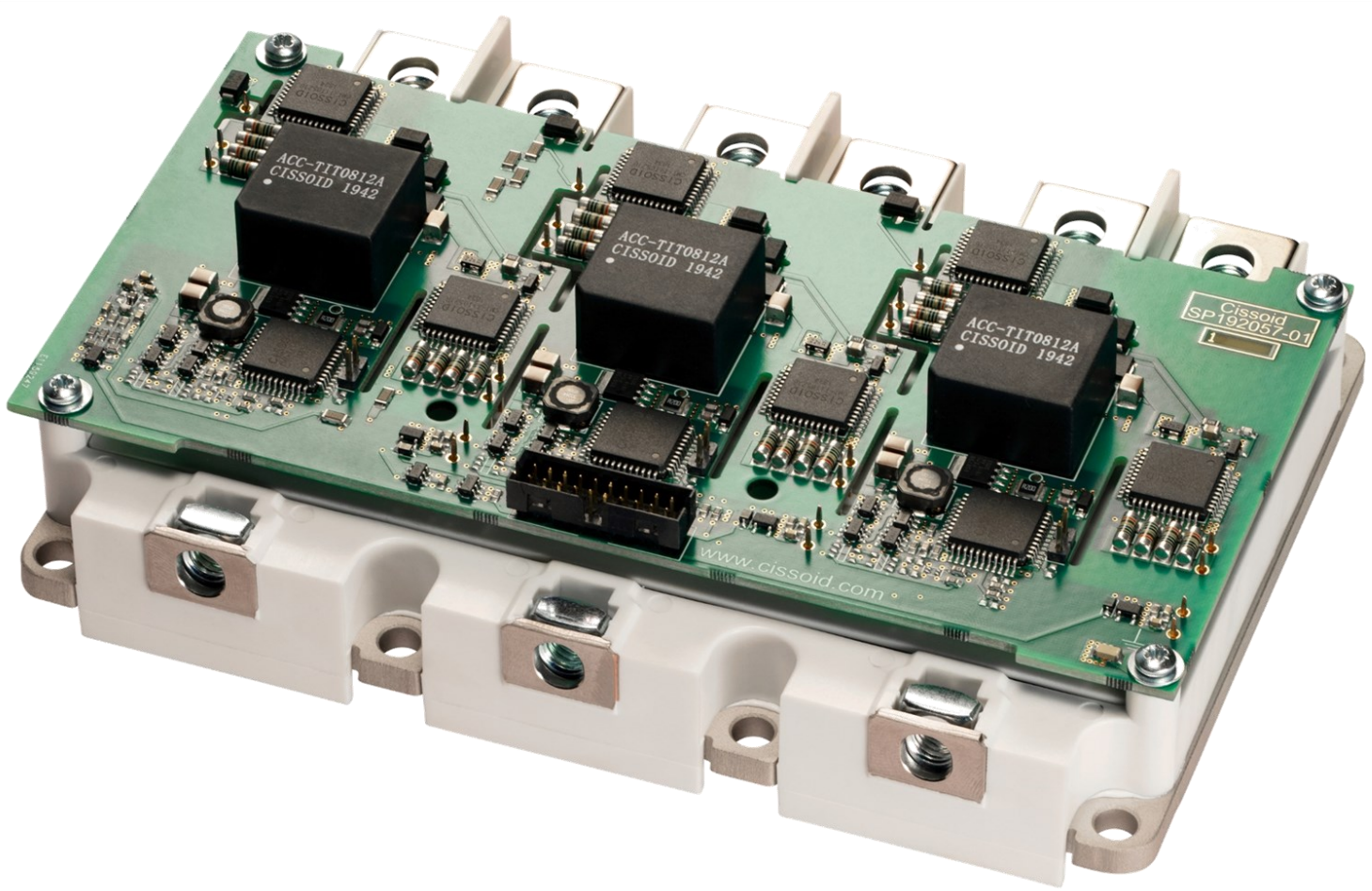


MOTOR CONTROL BOARD

Stacking the motor control board on top of the Intelligent Power Module (IPM) could further increase the thermal constraints by reducing air flow on gate driver board



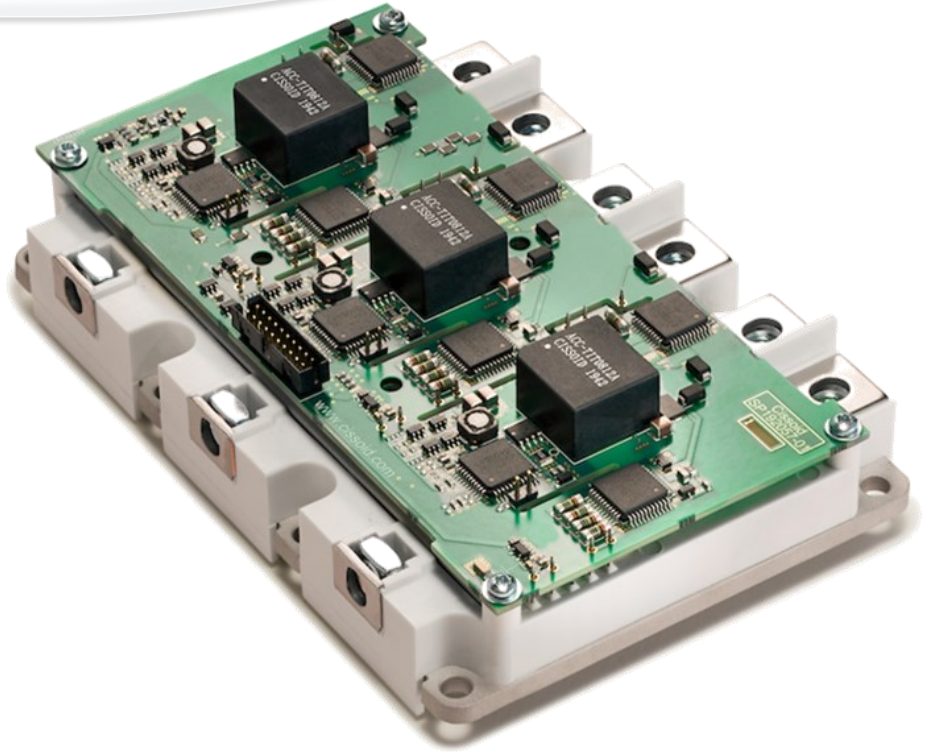
CISSOID/Silicon Mobility
OLEA® COMPOSER - T222
3-Phase 1200V/550A
SiC Inverter Starter Kit



GATE DRIVER/POWER MODULE CO-DESIGN

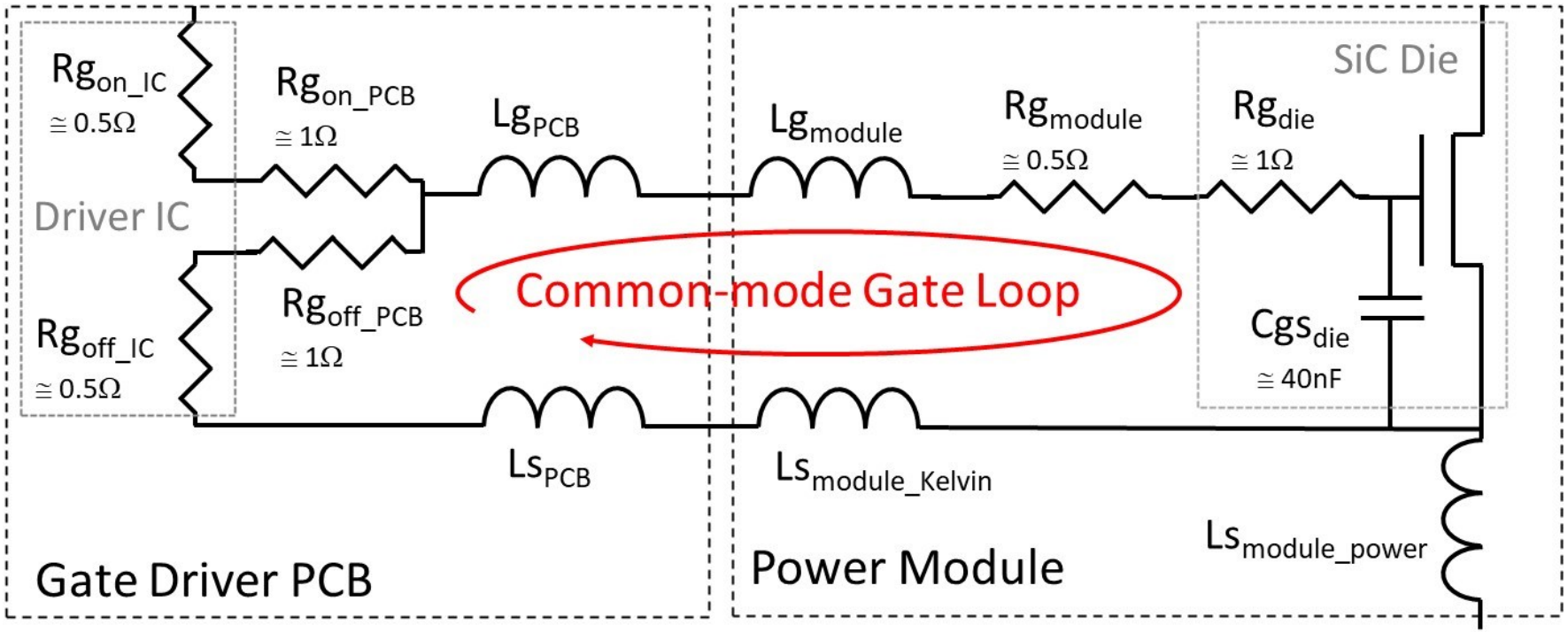
SiC Intelligent Power Modules (IPMs)

- They offer an optimized mechanical and electrical integration of the power module and its gate driver
- Particularly interesting for SiC Power Modules as the gate driver design is more challenging
  - Higher dV/dt and dI/dt
  - Gate loop inductances must be minimized
  - Higher isolation voltages
  - Higher thermal constraints
  - Desaturation detection should be carefully optimized



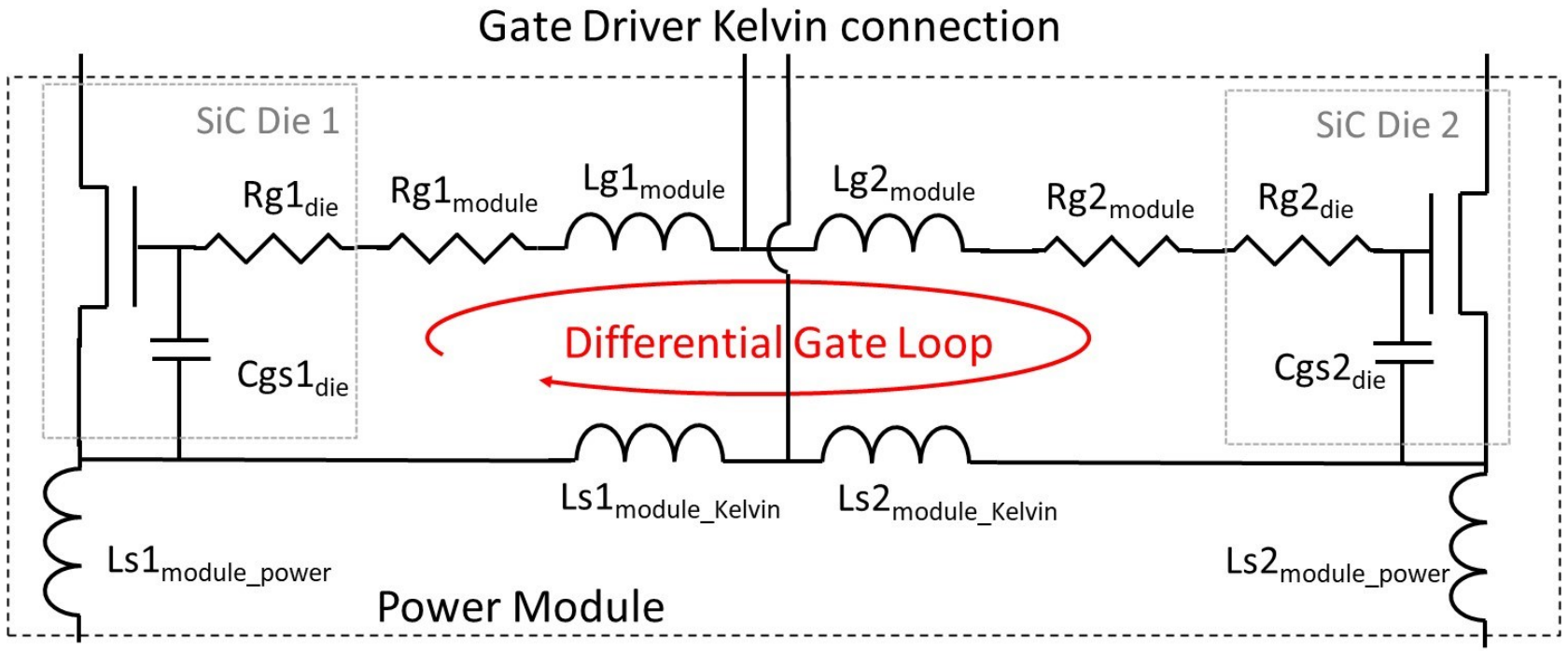
TRADE-OFF IN IPM THERMAL DESIGN

- Based on gate charge & dV/dt specifications, the gate resistor can be optimally distributed between the gate driver PCB and the power module to minimize gate driver self-heating



TRADE-OFF IN IPM THERMAL DESIGN

- Putting more gate resistance inside the power module also helps in damping oscillations in the differential gate loop [Ref 3]
- However, it reduces dV/dt tuning range at gate driver level



CONCLUSION

- Care should be taken in gate driver thermal design in high power density applications as
  - The ambient temperature (T_a) increases inside the power converter
  - High switching frequencies push up the gate driver board self-heating
  - The requirement to put the gate driver close to the power module to reduce parasitic inductances further increases thermal constraints
  - Losses neglected at lower voltage/frequency could become significant
- This can lead to the need to select high temperature components: gate driver IC's (T_{jmax} = 150°C … 175°C), PCB (high T_g), resistors …

REFERENCES

- [Ref 1] On Semi Application Note AND9596/D: “A Quick PCB Thermal Calculation for Power Electronic Devices with Exposed Pad Packages”

  https://www.onsemi.com/pub/Collateral/AND9596-D.PDF

- [Ref 2] Vishay Application Note: “Thermal Management in Surface-Mounted Resistor Applications”

  https://www.vishay.com/docs/28844/tmismra.pdf

- [Ref 3] F. Xu and L. Chen, "Suppressing Gate Voltage Oscillation in Paralleled SiC MOSFETs for HEV/EV Traction Inverter Application," 2019 IEEE Energy Conversion Congress and Exposition (ECCE), 2019, pp. 3548-3553, doi: 10.1109/ECCE.2019.8912638.

  https://ieeexplore.ieee.org/abstract/document/8912638

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