

CHT-74021 DATASHEET

Revision: 3.7
10-Dec-23
(Last Modified Date)

High-Temperature, Quad 2-Inputs NOR Gate

General Description

The CHT-74021 contains four independent 2-inputs NOR gates, performing the Boolean function :

$$Y = \overline{A + B}$$

This circuit is designed assuring latchup-free operation for all supply and temperature conditions.

The CHT-74021 can operate with supply voltages from 3.3 to 5V ($\pm 10\%$).

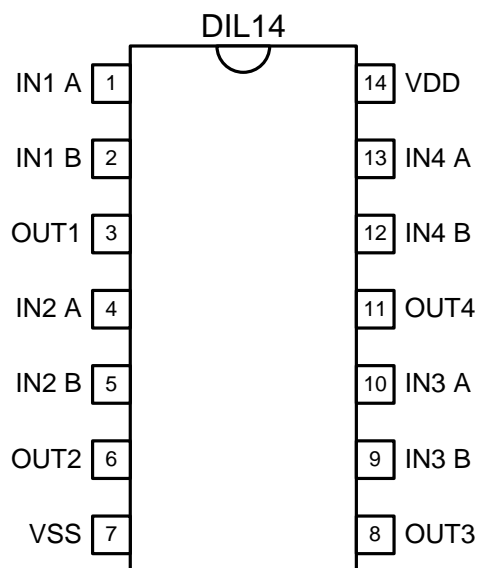
Features

- Qualified from -55 to +225°C (Tj)
- 3.3 to 5V ($\pm 10\%$) supply voltages
- Latchup-free at any supply and temperature condition
- Validated at 225°C for 30000 hours (CDIL14) and 20000 hours (CSOIC16) (and still on-going)
- Available in DIL14 and CSOIC16 hermetic standard package

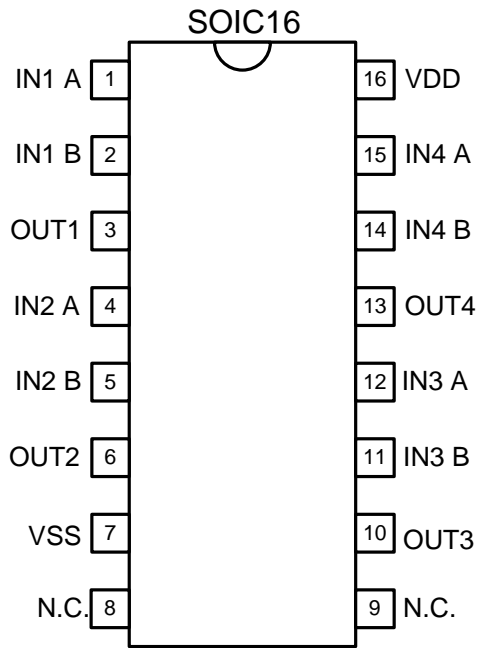
Applications

- Well logging,
- Automotive, Aeronautics & Aerospace
- Harsh Environments

Package and Pin Configuration



| Pin | Symbol | Description |
|-----|--------|-------------------------------------|
| 1 | IN1 A | Input A of the NOR gate number 1 |
| 2 | IN1 B | Input B of the NOR gate number 1 |
| 3 | OUT1 | Output of the NOR gate number 1 |
| 4 | IN2 A | Input A of the NOR gate number 2 |
| 5 | IN2 B | Input B of the NOR gate number 2 |
| 6 | OUT2 | Output of the NOR gate number 2 |
| 7 | VSS | Circuit core ground terminal. |
| 8 | OUT3 | Output of the NOR gate number 3 |
| 9 | IN3 B | Input B of the NOR gate number 3 |
| 10 | IN3 A | Input A of the NOR gate number 3 |
| 11 | OUT4 | Output of the NOR gate number 4 |
| 12 | IN4 B | Input B of the NOR gate number 4 |
| 13 | IN4 A | Input A of the NOR gate number 4 |
| 14 | VDD | Circuit core power supply terminal. |



| Pin | Symbol | Description |
|-----|--------|-------------------------------------|
| 1 | IN1 A | Input A of the NOR gate number 1 |
| 2 | IN1 B | Input B of the NOR gate number 1 |
| 3 | OUT1 | Output of the NOR gate number 1 |
| 4 | IN2 A | Input A of the NOR gate number 2 |
| 5 | IN2 B | Input B of the NOR gate number 2 |
| 6 | OUT2 | Output of the NOR gate number 2 |
| 7 | VSS | Circuit core ground terminal. |
| 8 | NC | Not connected |
| 9 | NC | Not connected |
| 10 | OUT3 | Output of the NOR gate number 3 |
| 11 | IN3 B | Input B of the NOR gate number 3 |
| 12 | IN3 A | Input A of the NOR gate number 3 |
| 13 | OUT4 | Output of the NOR gate number 4 |
| 14 | IN4 B | Input B of the NOR gate number 4 |
| 15 | IN4 A | Input A of the NOR gate number 4 |
| 16 | VDD | Circuit core power supply terminal. |

Function Table

| INPUT | | OUTPUT |
|-------|---|--------|
| A | B | Y |
| L | L | H |
| L | H | L |
| H | L | L |
| H | H | L |

Function and Logical Diagrams

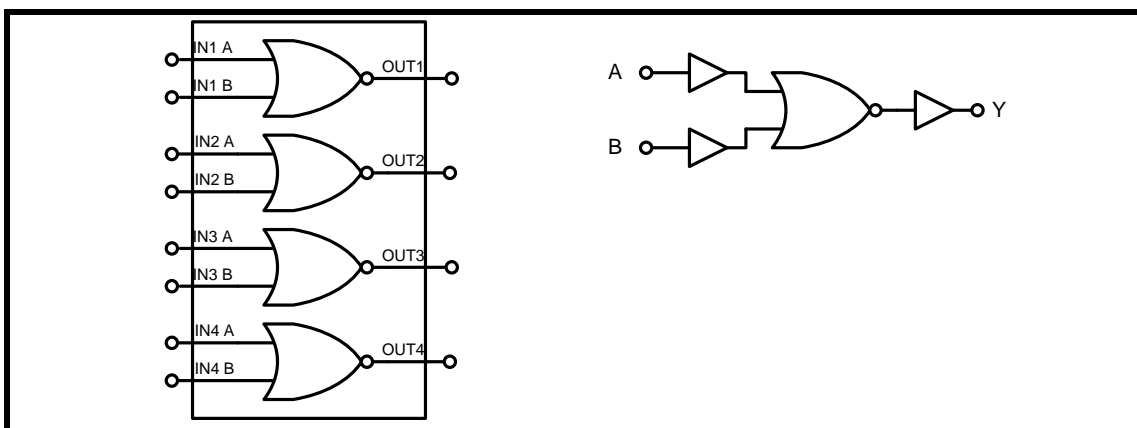


Figure 1. CHT-74021: simplified block diagram.

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND -0.5 to 6.0V
Voltage on any Pin to GND -0.5 to $V_{DD}+0.5V$

Operating Conditions

Supply Voltage V_{DD} to GND 3.3V to 5V ($\pm 10\%$)
Junction temperature -55°C to +225°C

ESD Rating (expected)

Human Body Model 1kV

DC Electrical Characteristics

Unless otherwise stated: $V_{DD}=5V$, $T_j=25^\circ C$. **Bold underlined** figures indicate values valid over the whole temperature range ($-55^\circ C < T_j < +225^\circ C$).

| Parameter | Condition | Min | Typ | Max | Units |
|--|---|-------------------|---------|-----------------------------------|-------|
| Supply voltage V_{DD} | | 2.97 | | 5.5V | V |
| Quiescent current I_{DD} | $V_{DD} = 3.3V$, $T_j = -55^\circ C$ | | | 4 | nA |
| | $V_{DD} = 5V$, $T_j = -55^\circ C$ | | | 13 | |
| | $V_{DD} = 3.3V$, $T_j = 225^\circ C$ | | | <u>2340</u> | |
| | $V_{DD} = 5V$, $T_j = 225^\circ C$ | | | <u>2550</u> | |
| Minimum HIGH level output voltage V_{OH} | $V_{DD} = 3.3V$, $I_{OH} < 4mA$ (source) | <u>2.7</u> | 3.04 | | V |
| | $V_{DD} = 5V$, $I_{OH} < 4mA$ (source) | <u>4.6</u> | 4.82 | | |
| Maximum LOW level output voltage V_{OL} | $V_{DD} = 3.3V$, $I_{OL} < 4mA$ (sink) | | 0.28 | <u>0.5</u> | V |
| | $V_{DD} = 5V$, $I_{OL} < 4mA$ (sink) | | 0.20 | <u>0.4</u> | |
| Minimum HIGH level input voltage V_{IH} | $V_{DD} = 3.3V$ | <u>2.4</u> | 2.10 | | V |
| | $V_{DD} = 5V$ | <u>3.7</u> | 3.49 | | |
| Maximum LOW level input voltage V_{IL} | $V_{DD} = 3.3V$ | | 1.72 | <u>1.5</u> | V |
| | $V_{DD} = 5V$ | | 2.16 | <u>2.0</u> | |
| Input leakage current (source / sink) $\pm I_i$ | $V_i = V_{CC}$ or GND, $V_{DD} = 3.3V$ | | ± 1 | <u>± 35</u> | nA |
| | $V_i = V_{CC}$ or GND, $V_{DD} = 5V$ | | ± 2 | <u>± 37</u> | |

AC Electrical Characteristics

Unless otherwise stated: VDD=5V, T_j=25°C. **Bold underlined** figures indicate values valid over the whole temperature range (-55°C < T_j < +225°C).

| Parameter | Condition | Temperature | Min | Typ | Max | Units |
|--|----------------------|-----------------------|-----|-----|------------------|-------|
| Propagation delay time from A or B to Y ¹ t _{PHL} | C _L =50pF | T _j =-55°C | | 9 | 12 | ns |
| | | T _j =25°C | | 11 | 14 | |
| | | T _j =225°C | | 15 | <u>19</u> | |
| Propagation delay time from A or B to Y t _{PLH} | C _L =50pF | T _j =-55°C | | 14 | 17 | ns |
| | | T _j =25°C | | 15 | 20 | |
| | | T _j =225°C | | 17 | <u>22</u> | |
| Output transition time High to Low t _{THL} | C _L =50pF | T _j =-55°C | | 13 | 17 | ns |
| | | T _j =25°C | | 14 | 18 | |
| | | T _j =225°C | | 17 | <u>22</u> | |
| Output transition time High to Low t _{TLH} | C _L =50pF | T _j =-55°C | | 19 | 25 | ns |
| | | T _j =25°C | | 20 | 26 | |
| | | T _j =225°C | | 23 | <u>30</u> | |

¹ Input A is 1% to 2% faster than input B.

AC Electrical Characteristics (cntd)

Unless otherwise stated: $V_{DD}=3.3V$, $T_j=25^\circ C$. **Bold underlined** figures indicate values valid over the whole temperature range ($-55^\circ C < T_j < +225^\circ C$).

| Parameter | Condition | Temperature | Min | Typ | Max | Units |
|---|------------|-------------------|-----|-----|------------------|-------|
| Propagation delay time from A or B to Y t_{PHL} | $C_L=50pF$ | $T_j=-55^\circ C$ | | 18 | 24 | ns |
| | | $T_j=25^\circ C$ | | 19 | 27 | |
| | | $T_j=225^\circ C$ | | 23 | <u>37</u> | |
| Propagation delay time from A or B to Y t_{PLH} | $C_L=50pF$ | $T_j=-55^\circ C$ | | 17 | 23 | ns |
| | | $T_j=25^\circ C$ | | 19 | 26 | |
| | | $T_j=225^\circ C$ | | 23 | <u>35</u> | |
| Output transition time High to Low t_{THL} | $C_L=50pF$ | $T_j=-55^\circ C$ | | 20 | 26 | ns |
| | | $T_j=25^\circ C$ | | 21 | 28 | |
| | | $T_j=225^\circ C$ | | 27 | <u>36</u> | |
| Output transition time High to Low t_{TLH} | $C_L=50pF$ | $T_j=-55^\circ C$ | | 23 | 30 | ns |
| | | $T_j=25^\circ C$ | | 24 | 32 | |
| | | $T_j=225^\circ C$ | | 26 | <u>34</u> | |

AC Waveforms

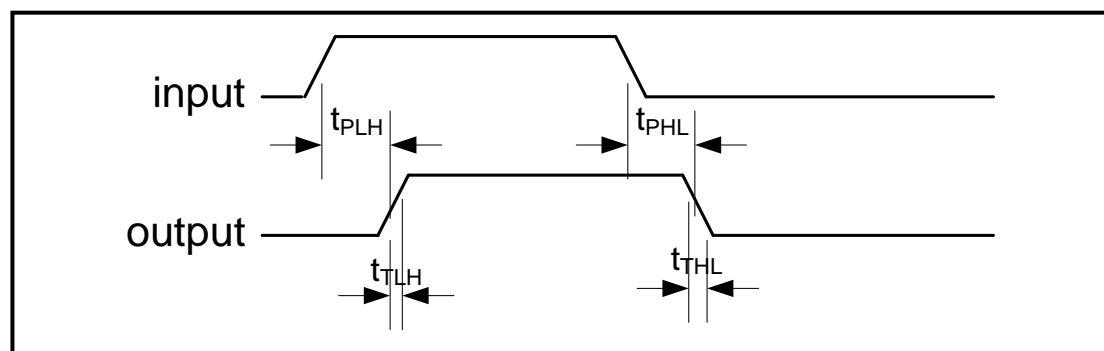
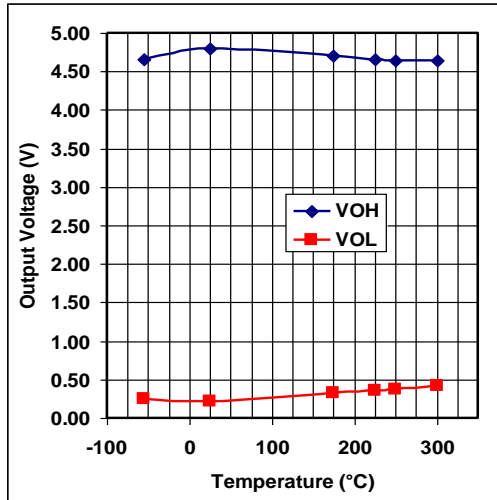
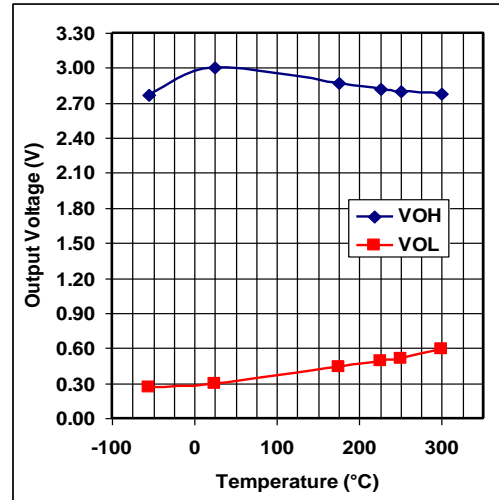


Figure 2. AC Waveforms

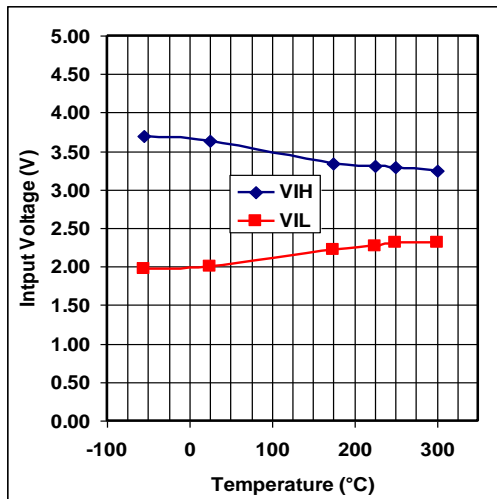
Typical Performance Characteristics



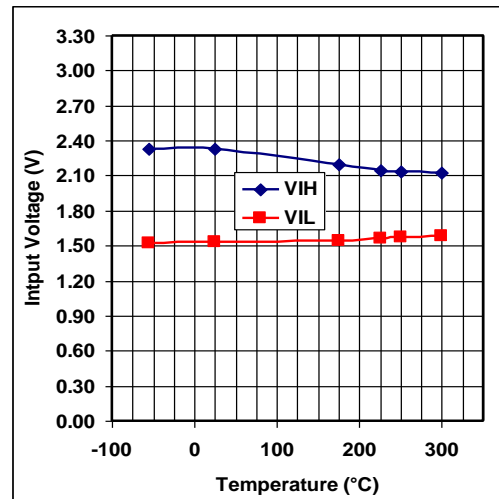
Output voltage levels versus temperature, $V_{DD} = 5V$



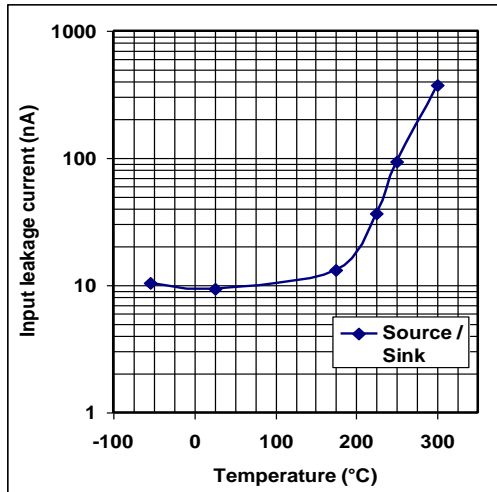
Output voltage levels versus temperature, $V_{DD} = 3.3V$



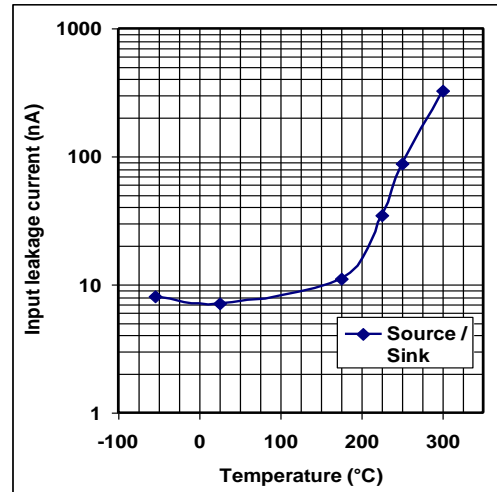
Input voltage levels versus temperature, $V_{DD} = 5V$



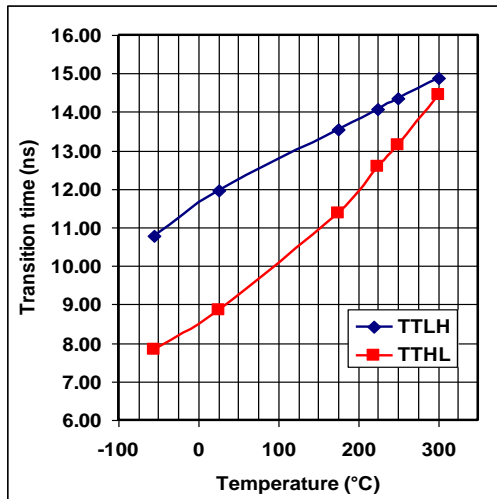
Input voltage levels versus temperature, $V_{DD} = 3.3V$



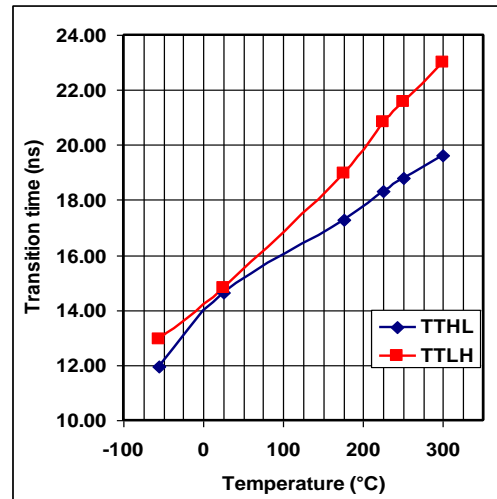
Input leakage current versus temperature,
 $V_{DD} = 5V$



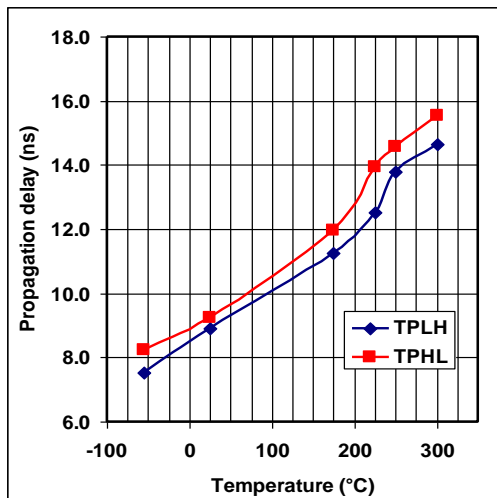
Input leakage current versus temperature,
 $V_{DD} = 3.3V$



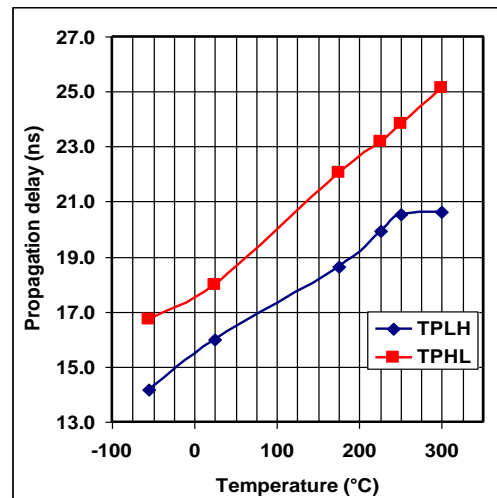
Transition times versus temperature,
 $V_{DD} = 5V$



Transition times versus temperature,
 $V_{DD} = 3.3V$



Propagation delays versus temperature,
 $V_{DD} = 5V$

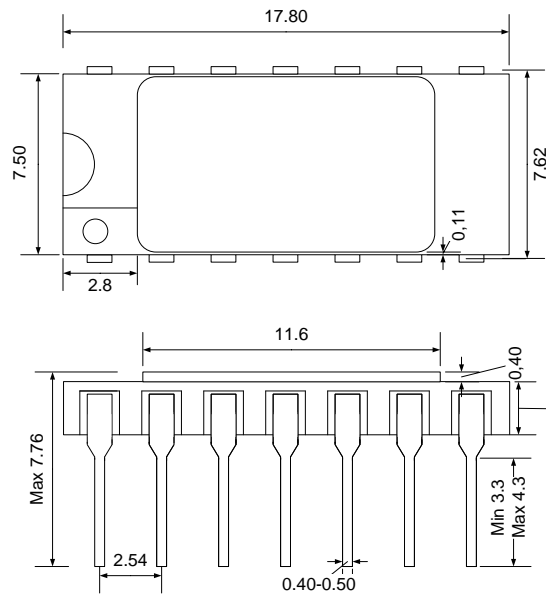


Propagation delays versus temperature,
 $V_{DD} = 3.3V$

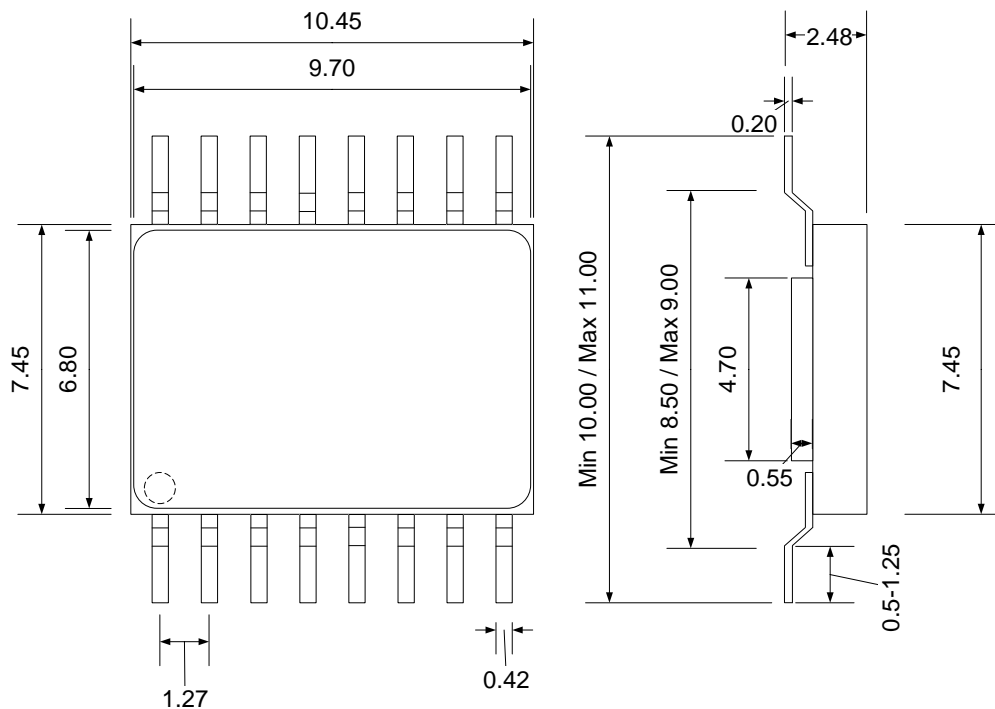
Ordering Information

| Ordering Reference | Package | Temperature Range | Marking | Status |
|---------------------|----------------|-------------------|-----------|--------------------|
| CHT-74021-CDIL14-T | Ceramic DIL14 | -55°C to +225°C | CHT-74021 | Not for new design |
| CHT-74021-CSOIC16-T | Ceramic SOIC16 | -55°C to +225°C | CHT-74021 | |

Package Dimensions



Drawing CDIL14 (mm +/- 10%)



Drawing CSOIC16 (mm +/- 10%)

Contact & Ordering

CISSOID S.A.

| | |
|---------------------------------------|--|
| Headquarters and contact EMEA: | CISSOID S.A. – Rue Francqui, 11 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: sales@cissoid.com |
| Representatives | Visit our website: www.cissoid.com |

Disclaimer

Neither CISSOID, nor any of its directors, employees or affiliates make any representations or extend any warranties of any kind, either express or implied, including but not limited to warranties of merchantability, fitness for a particular purpose, and the absence of latent or other defects, whether or not discoverable. In no event shall CISSOID, its directors, employees and affiliates be liable for direct, indirect, special, incidental or consequential damages of any kind arising out of the use of its circuits and their documentation, even if they have been advised of the possibility of such a damage. The circuits are provided "as is". CISSOID has no obligation to provide maintenance, support, updates, or modifications.