CHT-ATLAS

Version: 3.6
20-Dec-23
(Last Modification Date)

Dual Channel Power Transistor Driver

General description

CHT-ATLAS is a high-temperature, high reliability power transistor driver integrated circuit specifically designed to drive wide-bandgap power transistors, in particular Gallium Nitride (GaN) and Silicon Carbide (SiC) devices including normally-On and normally-Off JFETs, MOSFETs and BJTs. It is also used with standard silicon MOSFETs and IGBTs in standard temperature applications (e.g. 125°C) where it brings an increase in reliability and lifetime by an order of magnitude compared to traditional solutions. The circuit features 2 independent push-pull channels capable of sourcing/sinking 2A each. When configured together to drive a single power switch, the combination of the 2 distinct channels allows driving of specific devices that require for instance a dynamic pulse of current in combination with a continuous current in order to be properly turned-on. The circuit includes a soft-shut-down capability that slowly shuts down the power transistor in case of fault.

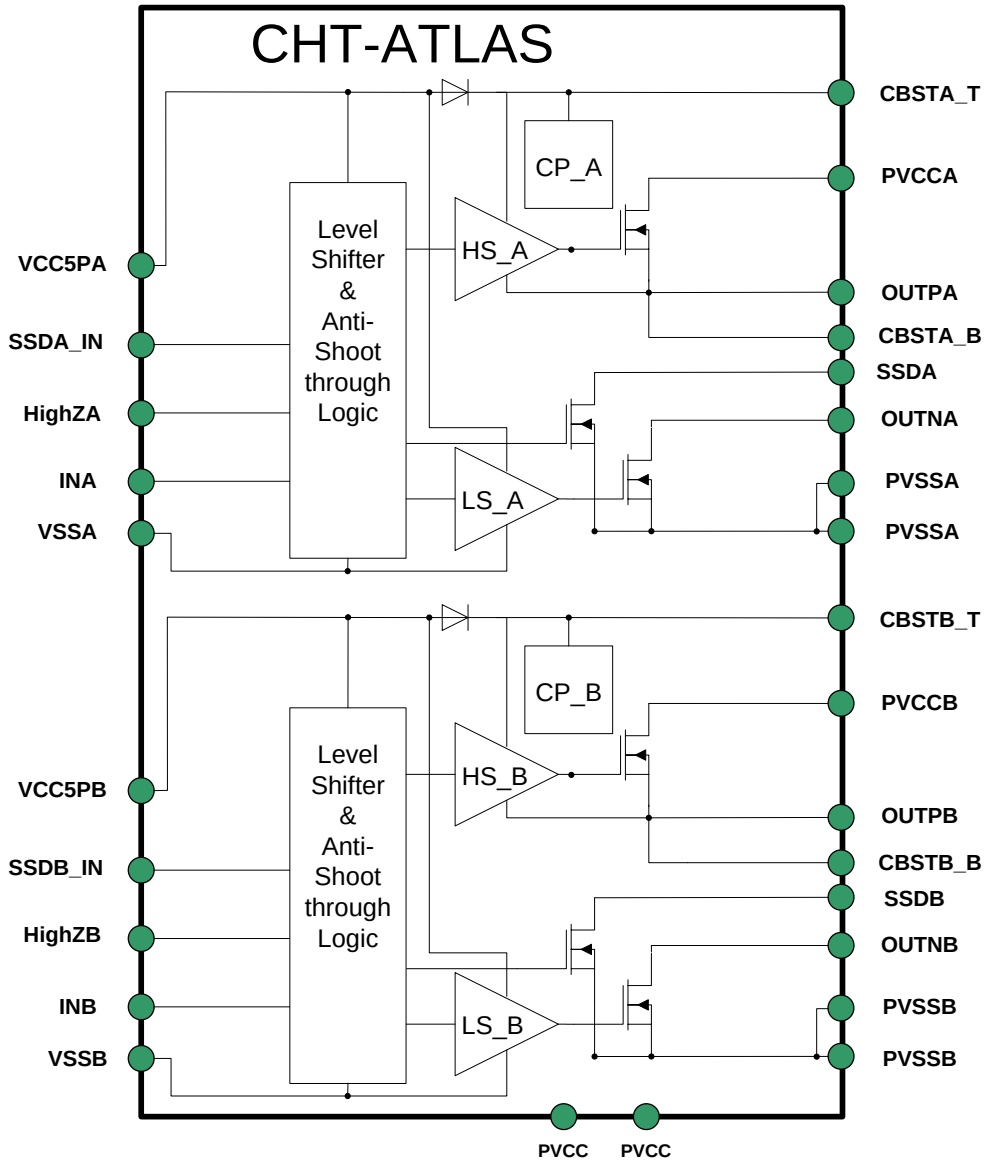
Features

- Operating junction temperature: from -55°C to +225°C
- Gate drive supply voltage: 5 to 30V
- 2 channels
- Separate logic level control inputs
- Output current: up to 2 x ±2A @ 225°C
- Propagation delay: 40 ns typ
- Rise time / fall time: 10ns Typ. (with C_{Load}=1nF and V_{CC}=15V)
- Soft-shut down
- High Impedance mode
- Capable to drive normally-On and normally-Off devices
- Validated at 225°C for 1000 hours (and still on-going)
- Package: CSOIC28

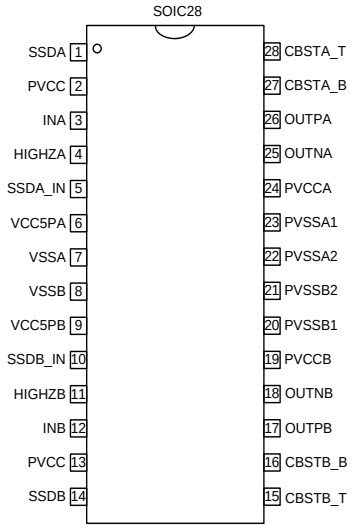
Applications

- Intelligent Power Modules (IPM)
- Power conversion, power generation and actuator controls in aeronautics
- Solar inverters
- Motor drives, battery chargers and DC-DC converters in EV / HEV
- Power conversion and motor drive in railway
- Switched mode power supplies (SMPS)
- Wind turbine power converters

Functional Block Diagram



Package Configuration and Pin Description:



Pin #	Pin Name	Pin Description
1	SSDA	Soft Shutdown output pin of channel A. When SSDA_IN pin is low, this node is pulled down to PVSSA.
2	PVCC	To be connected to PVCCA and PVCCB
3	INA	Schmitt triggered input of channel A driver. 5V CMOS input with respect to VSS.
4	HIGHZA	Schmitt triggered input of the tri-state control signal for channel A driver. 5V CMOS input with respect to VSSA. When driven low, sink, source and SSDA output transistors are turned off (see ATLAS Logic Table). Channel A output is in high impedance.
5	SSDA_IN	Schmitt triggered input controlling the soft shut-down transistor for the channel A (see ATLAS Logic Table)
6	VCC5PA (input)	5V positive power supply with respect to VSSA. To be bypassed to VSSA by a 1µF capacitor.
7	VSSA	Analogue negative power supply for channel A
8	VSSB	Analogue negative power supply for channel B
9	VCC5PB (input)	5V positive power supply with respect to VSSB. To be bypassed to VSSB by a 1µF capacitor.
10	SSDB_IN	Schmitt triggered input controlling the soft shut-down transistor for the channel B (see ATLAS Logic Table)
11	HIGHZB	Schmitt triggered input of the tri-state control signal for Channel B driver. 5V CMOS input with respect to VSSB. When driven low, both sink and source output transistors are turned off. Channel B output is in high impedance.
12	INB	Schmitt triggered input of Channel B driver. 5V CMOS input with respect to VSSB.
13	PVCC	To be connected to PVCCA and PVCCB
14	SSDB	Soft Shutdown output pin of channel B. When SSDB_IN pin is low, this node is internally pulled down to PVSSB.
15	CBSTB_T	Connection for the top plate of the bootstrap capacitor for channel B
16	CBSTB_B	Connection for the bottom plate of the boot-strap capacitor for channel B
17	OUTPB	Channel B sourcing output (Isource_max=2A)
18	OUTNB	Channel B sinking output (Isinking_max=2A)
19	PVCCB	Positive power supply of channel B driver.
20	PVSSB1	Negative power supply for channel B (First Pin)
21	PVSSB2	Negative power supply for channel B (Second Pin[1])
22	PVSSA2	Negative Power supply for channel A (Second Pin[2])
23	PVSSA1	Negative power supply for channel A (First Pin)
24	PVCCA	Positive power supply for channel A.
25	OUTNA	Channel A sinking output (Isinking_max=2A)
26	OUTPA	Channel A sourcing output (Isource_max=2A)
27	CBSTA_B	Connection for the bottom plate of the boot-strap capacitor for channel A
28	CBSTA_T	Connection for the top plate of the bootstrap capacitor for channel A

[1]To minimize parasitic inductors and ringing, both PVSSB1 and PVSSB2 must be connected to the negative power supply with minimum parasitic inductors

[2] To minimize parasitic inductors and ringing, both PVSSA1 and PVSSA2 must be connected to the negative power supply with minimum parasitic inductors

Logic Table

Inputs			Outputs		
INA(B)	SSDA_IN (SSDB_IN)	HIGHZA(B)	OUTPA(B)	OUTNA(B)	SSDA(B)
0	1	1	highZ	PVSSA	highZ
1	1	1	PVCCA	highZ	highZ
X	0	1	highZ	highZ	PVSSA
X	X	0	highZ	highZ	highZ

In normal operation pins HIGHZA/B and pins SSDA/B_IN are set to logic-1 (VCC5PA/B=5V). Applying logic-0 (0V) to pin INA/B turns the low-side driver on, pulling pin OUTA/B down to PVSSA/B. OUTPA/B is in high-impedance state. Applying logic-1 (5V) to pin INA/B, pin OUTNA/B is set to high-impedance state while the high-side driver is turned on pulling OUTPA/B to PVCCA/B.

Maintaining the device enabled (HIGHZA/B set to logic-1) the soft-shutdown is activated by setting pin SSDA/B_IN to logic-0. Both high-side and low-side drivers are turned off setting pints OUTPA/B and OUTNA/B to high impedance state. SSDA/B pin is pulled down to PVSSA/B. The logic level at pin INA/B does not matter.

The device is disabled when pin HIGHZA/B is set to logic-0, whatever the logic level at the other control signals.

Absolute Maximum Ratings

These ratings are considered individually (not in combination). If not specified, voltages are related to VSSA for channel A and to VSSB for channel B. VSSA and VSSB must be at the same potential.

Supply Voltage PVCCA/B to PVSSA/B	-0.5 to 35V
Supply Voltage VCC5PA/B to VSSA/B	-0.5 to 5.5V
Voltage on IN, HIGHZ, SSD_IN to VSS	-0.5 to VCC5P+0.5V
Voltage on CBST_T to PVSS	VCC5P-0.5 to PVCC+5.5
Driver Output voltage (OUT, CBST_B)	PVSS-0.5 to PVCC+5.5
Junction temperature T_j	250°C

ESD Rating (expected)

Human Body Model	1.5kV

Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Frequent or extended exposure to absolute maximum rating conditions or above may affect device reliability.

Operating Conditions

Supply Voltage VCC5P to VSS	4.75V to 5.25V
Supply Voltage PVCC to PVSS	5V to 30V
Junction temperature	-55°C to +225°C

Electrical Characteristics

Unless otherwise stated: (VCC-VSS)=5V, (PVCC-PVSS)=15V, T_j=25°C. **Bold underlined** values indicate values over the whole temperature range (-55°C < T j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
External Power Supply					
External Power Supply[3] PVCCA/B versus PVSS		5		30	V
PVCCA/B quiescent current	INA/INB=0			**0.1**	mA
PVCCA/B quiescent current	INA/INB=5V			**0.2**	mA
PVCCA/B average current	20kHz, 50% duty cycle PVCCA/B = 25V C_{LOAD} = 1nF			**0.4**	mA
VCC5PA/B quiescent current	INA/INB=0 and HighZA/B=X			**0.1**	mA
VCC5PA/B quiescent current	INA/INB=X and HighZA/B=0			**0.1**	mA
VCC5PA/B quiescent current[4]	INA/INB=5V and HighZA/B=5V			**1**	mA
VCC5PA/B average current	20kHz, 50% duty cycle			**0.5**	mA
External Power Supply VCC5P versus VSS		4.75		5.25	V
Input signals (INA/B, HighZA/B)					
Input start threshold		**3.03**	3.43	**3.83**	V
Input stop threshold		**1.1**	1.39	**1.85**	V
Hysteresis		**1.68**	2.04	**2.39**	V
Drivers					
OUTNA/B sink current[5]		**2**			A
OUTPA/B source current[6]		**1.95**			A
High state output resistance				**2.1**	Ω
Low state output resistance				**2**	Ω
Propagation delay when output rising (IN→OUTPA/B)	CLoad=1nF; (PVCC-PVSS)=15V (50%→ 50%)		40		ns
Propagation delay when output falling (IN→OUTNA/B)	CLoad=1nF; (PVCC-PVSS)=15V (50%→ 50%)		40		ns
Rise Time (10%-90%)	CLoad=1nF; (PVCC-PVSS)=15V		10		ns
Fall Time (10%-90%)	CLoad=1nF; (PVCC-PVSS)=15V		10		ns
Soft Shut-down outputs (SSDA/B)					
Delay from SSDA/B_IN to SSDA/B output			120		ns
Open-drain transistor ON-Resistance		**15**	35	**65**	Ω
Thermal resistance					
Junction–to-air thermal resistance (Θ_{JA})			42		°C/W

[3] Voltage externally supplied to the chip

[4] In this case, quiescent current means the average current over several Charge-Pump turn-on/off periods

[5] In practice, the maximum sink current is N multiplied by the number of ATLAS channels used in the application

[6] In practice, the maximum source current is N multiplied by the number of ATLAS channels used in the application

Typical Performance Characteristics

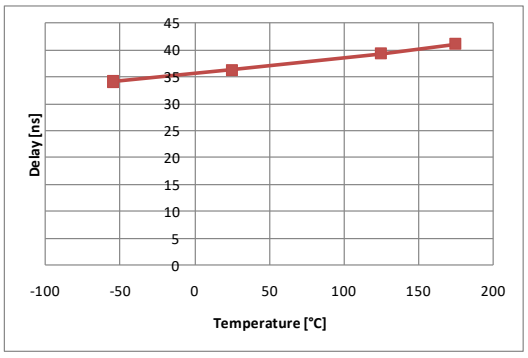


Figure 1: Turn-Low Propagation Delay vs. Temperature

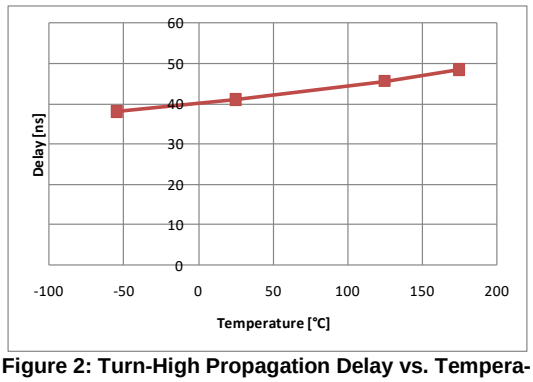


Figure 2: Turn-High Propagation Delay vs. Temperature

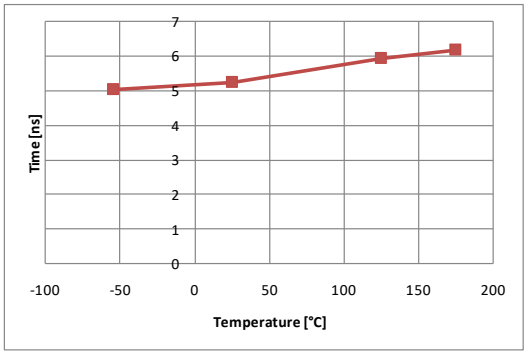


Figure 3: Turn-Low Fall Time vs. Temperature

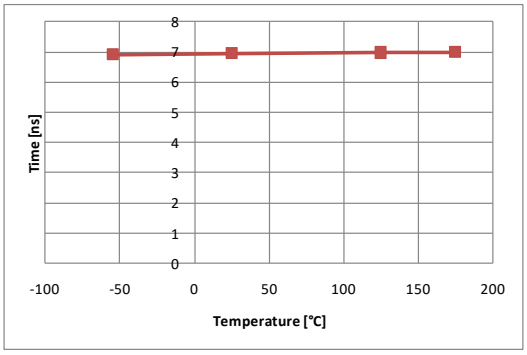


Figure 4: Turn-High Rise Time vs. Temperature

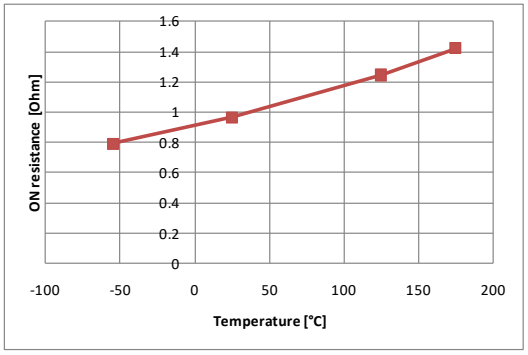


Figure 5: Low-state output resistance vs. Temperature

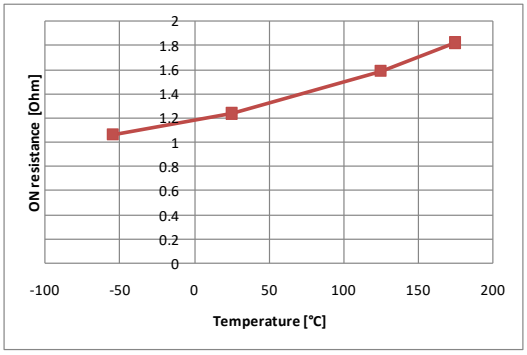


Figure 6: High-state output resistance vs. Temperature

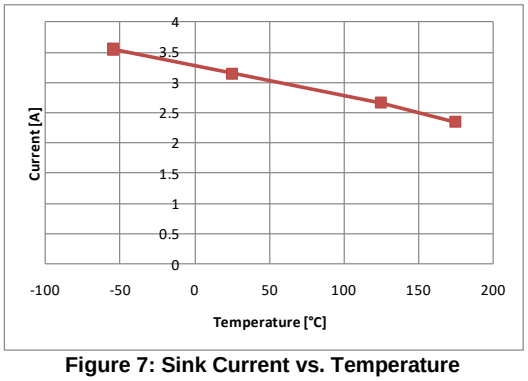


Figure 7: Sink Current vs. Temperature

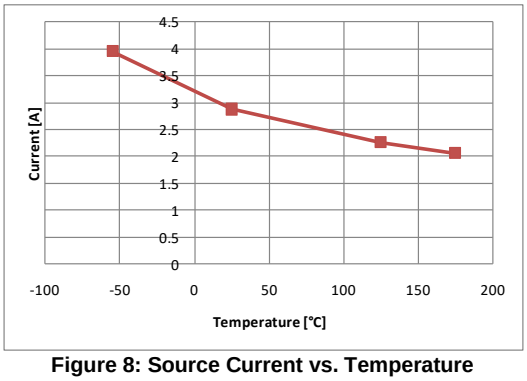
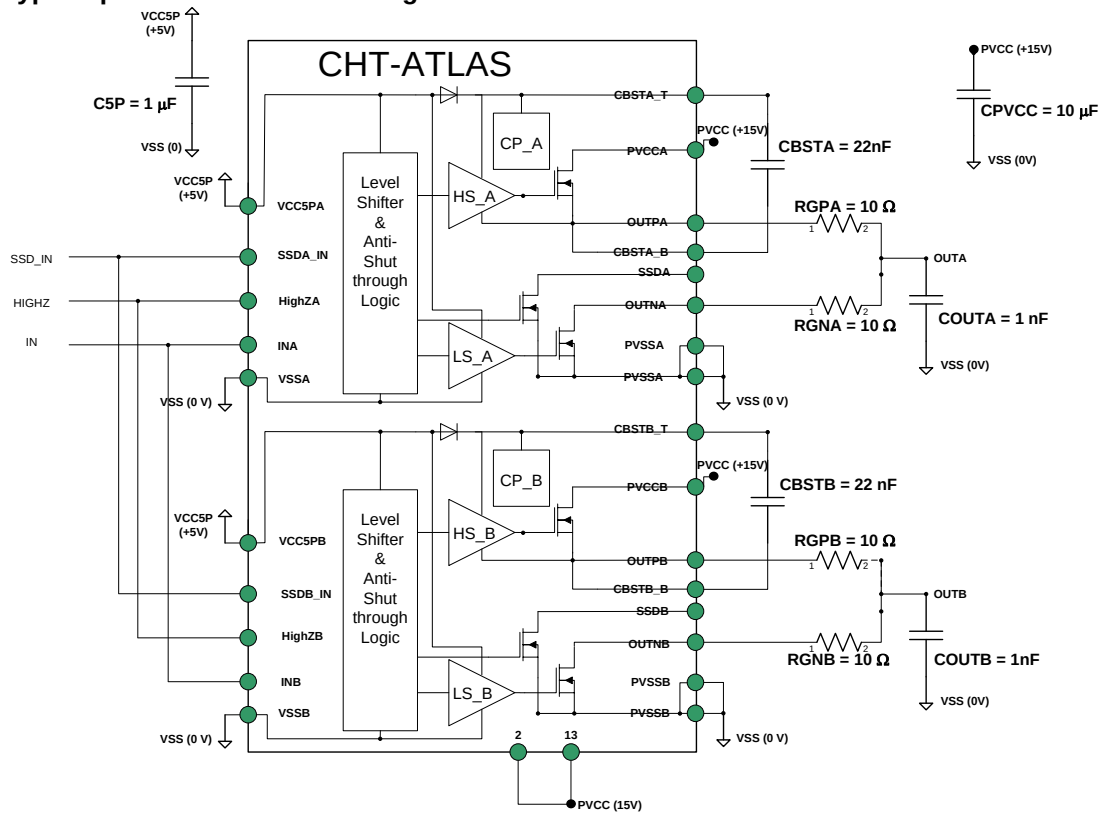


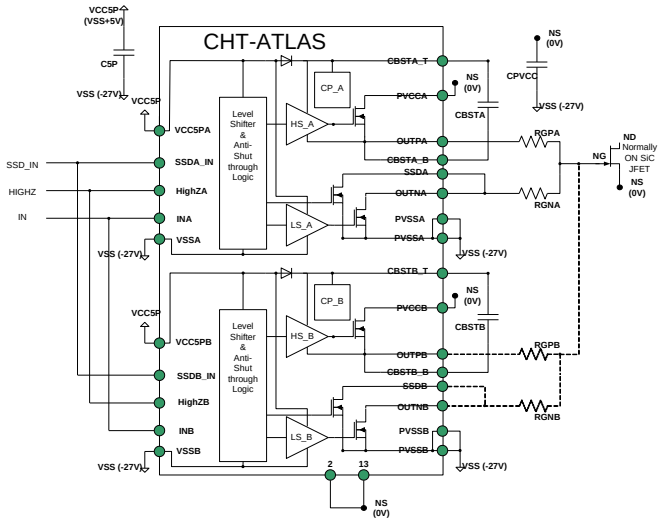
Figure 8: Source Current vs. Temperature

Typical performances: Switching Times Test Circuit



Application Diagrams

Driving a Normally-ON SiC JFET



The normally-ON SiC JFET is turned off once the gate-source voltage drops below the negative pinch-off voltage of the JFET. At zero gate-source voltage, the device is fully ON. For proper gate drive, CHT-ATLAS has its positive supply pins (PVCCA/B) tied to the source of the JFET (NS). Its negative supply pins (PVSSA/B) are connected to a negative voltage power supply with respect to NS.

The logical control signals (INA/B, HIGHZA/B, SSDA/B_IN) belong to the VCC5P supply domain (5V with respect to VSS). VSS and PVSS must be electrically tied together in the application board.

Local decoupling between PVCC(=NS) and PVSS is mandatory as large current peaks flow through those supply connections during gate switching. The decoupling capacitor must deliver the total gate charge with minimum supply voltage loss.

CHT-ATLAS features 2 channels (A and B) with equal drive capabilities (>2A, <2Ω). For higher drive capability, the channels can be connected in parallel.

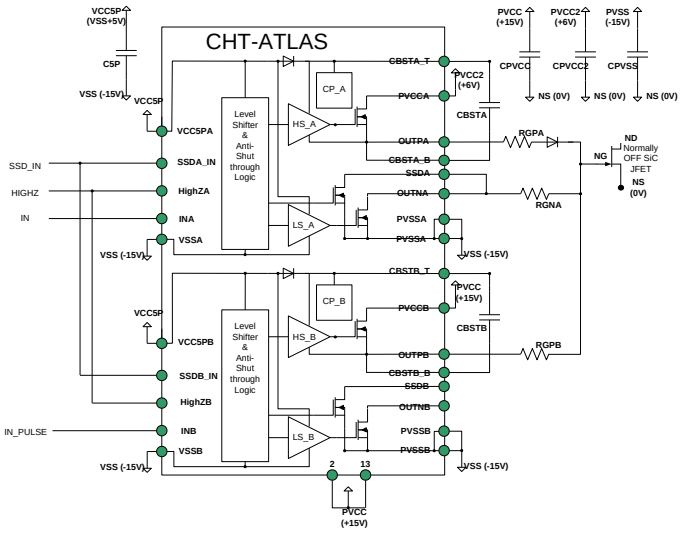
The high-side (pins OUTPA/B) and low-side (pin OUTNA/B) drivers inside CHT-ATLAS pull the JFET gate voltage up and down through series resistors RGPA/B and RGNA/B

Resistors RGPA/B and RGNA/B limit the gate current at turn-on and turn-off and control the switching time of the JFET and therefore the dV/dt in order to reduce probability of shoot-through current (parasitic turn-on of the blocking device in a half-bridge configuration). They also help damping oscillations and limiting voltage overshoot at the JFET gate which could result from stray inductances in the gate drive circuit and which could cause damage to the devices. Typical values range from 5 to 10 ohms.

At positive switching, the bootstrap capacitors CBSTA/B bias the high-side drivers above the positive supply voltage PVCC. The typical bootstrap capacitance is 22nF. After the transition, the internal charge-pumps keep the high-side drivers on till the next negative transition without any minimum switching frequency constraint.

SSDA/B offer soft-shutdown of the JFET by controlling the input signal SSDA/B_IN. Both high-side and low-side drives are turned off and the gate is pulled down through RGNA/B via pin SSDA/B by weaker pull-down transistors.

Driving a Normally-OFF SiC JFET



Unlike the normally-on JFET, the gate-source junction of the normally-off SiC JFET is forward biased in the device conduction state. In addition to the dynamic current for charging/discharging the total gate capacitance, some steady-state current has to be provided to maintain conduction after the device has been switched on.

The two channels of CHT-ATLAS are combined in a way to deliver both dynamic and steady-state currents.

Channel A must be driven with the regular PWM control signal (IN) while channel B must be driven by a second control signal (IN_PULSE) giving a shorter impulse at the turn-on.

The dynamic current is supplied by the high-side driver of channel B (OUTPB) at turn-on and the low-side driver of channel A (OUTNB) at turn-off through resistances RGPB and RGNA.

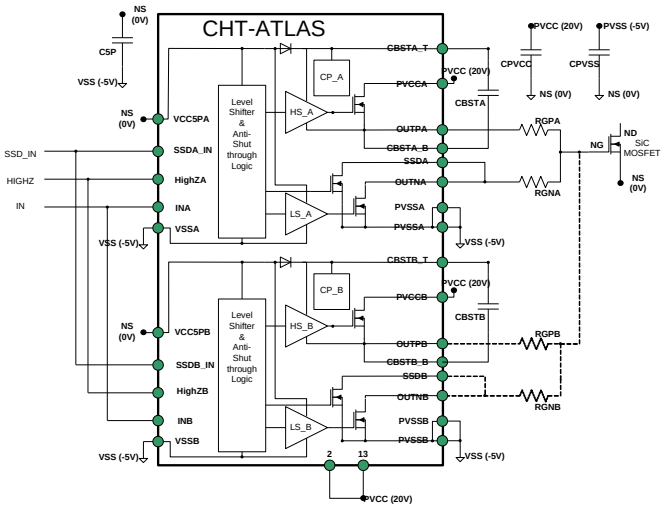
The steady-state current is provided by the high-side driver in channel A (OUTPA). Similar considerations as with the normally-on JFET apply to the selection of resistors RGPA and RGPB. Avoiding too small value for RGPB, the positive supply voltage PVCCB is typically +15V[7].

The threshold voltage of the normally-off JFET being low, the gate should best be pulled down to a negative voltage with respect to the JFET source when the device is turned off. The lower the voltage, the better the immunity to shoot-through current in a half-bridge application. The negative supply PVSS depends on the SiC device gate-source voltage rating. A typical assumption for PVSS is -15V.

The steady-state current is supplied by the positive supply of channel A (PVCC2) through pin OUTPA and resistor RGPA. RGPA and PVCC2 must be sized in order to deliver the current required by the SiC device which is of the order of 100mA7. PVCC2 can be identical to PVCC but a smaller voltage could be used for power saving, a diode must then be inserted between RGPA and the gate of the SiC device.

Local decoupling of PVCC, PVCC2 and PVSS to NS is mandatory.

Driving a SiC MOSFET



Driving a SiC MOSFET requires a gate driver capable of a large gate voltage swing and fast gate voltage transitions.

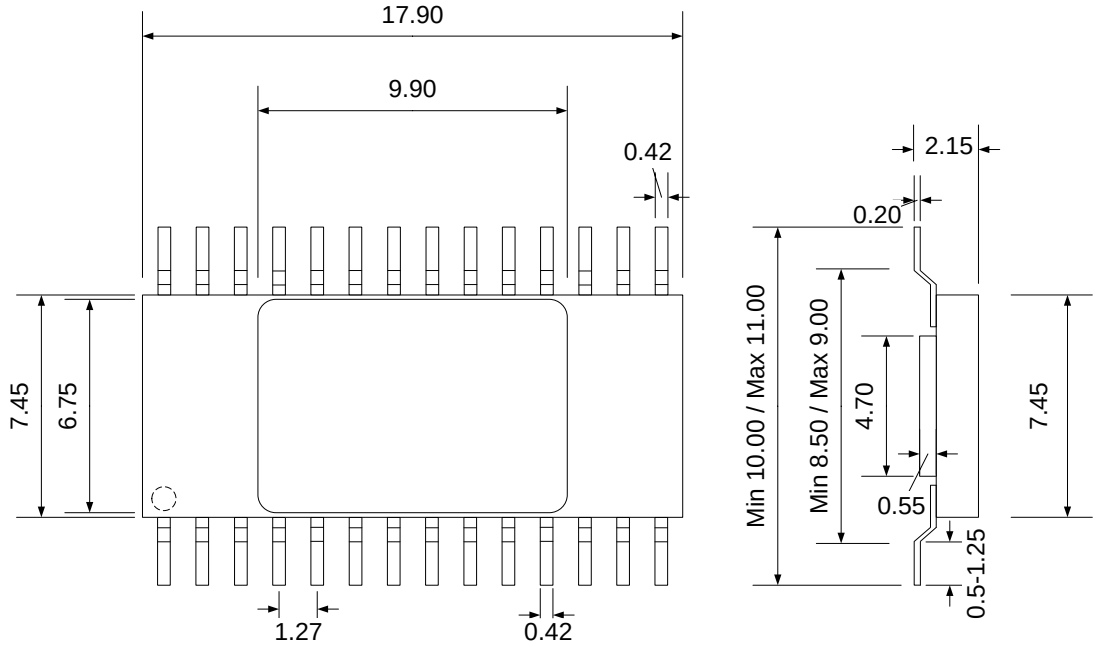
Both CHT-ATLAS channels can be connected in parallel for fast gate switching.

The high-side driver pulls the MOSFET gate voltage to PVCC (typically 20 V for best performance[8]) and the low-side divers pulls it down to negative PVSS8 (typically -2V to -5V).

Considerations similar to those mentioned with SiC JFETS apply with respect to the gate resistances and the importance of proper decoupling of the supplies.

[7] Robin Kelley et al., “Optimized Gate Driver for Enhancement-mode SiC JFET”
[8] Bob Callanan, “Application Considerations for SiC MOSFETS”, Cree Inc., January 2011.

Package Drawing



CSOIC 28 Drawing (mm +/- 10%)

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-TIT3345E-CSOIC28-T	CSOIC-28	-55°C to +225°C	CHT-TIT3345E

Contact & Ordering

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