CHT-74-4040-DATASHEET

Version: 1.6
21-Dec-23
(Last Modification Date)

High Temperature,12 stage binary counter

General Description

The CHT-74-4040 is a 12-stage asynchronous binary counter.

The device is incremented on the falling edge (negative transition) of the CLOCK input. All the outputs are reset to a low level by applying a logical high on the CLEAR input.

In frequency divider applications, the clock can be divided by up to 4096.

The device is pin compatible with the industry standards 74xx4040, / CD4040. As such, CISSOID CHT-74-4040 can replace advantageously the above devices and bring a lifetime increase of 1 to 2 decades depending on the temperature range; it also increases the operating temperature capability to -55°~+225°C which cannot be achieved by traditional products.

The CHT-74-4040 can operate with supply voltages from 3.3 to 5V (±10%).

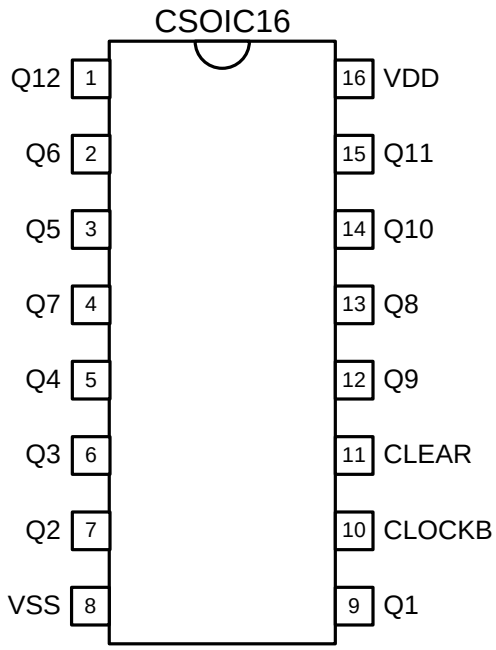
Features

- Functional from -55 to +225°C (Tj)
- 3.3 to 5V (±10%) supply voltages
- Latchup-free at any supply and temperature condition
- Available in CSOIC16 hermetic standard package
- Typical propagation delay: 19 ns
- Low quiescent current: 21µA Max (@225°C, 5V)
- Output drive capability: 4mA Max
- Validated at 225°C for 1000 hours (and still on-going)

Applications

- Clock generation
- Frequency division

Package and Pin Configuration



Pin	Symbol	Description
1	**Q12**	Parallel output <12>
2	**Q6**	Parallel output <6>
3	**Q5**	Parallel output <5>
4	**Q7**	Parallel output <7>
5	**Q4**	Parallel output <4>
6	**Q3**	Parallel output <3>
7	**Q2**	Parallel output <2>
8	**VSS**	Negative power supply
9	**Q1**	Parallel output <1>
10	**CLOCKB**	Clock input (HIGH to LOW, edge triggered)
11	**CLEAR**	Reset input (active HIGH)
12	**Q9**	Parallel output <9>
13	**Q8**	Parallel output <8>
14	**Q10**	Parallel output <10>
15	**Q11**	Parallel output <11>
16	**VDD**	Positive power supply

Function Table

CLOCKB	CLEAR	OUTPUT STATE
X	H	All “LOW”
Rising edge	L	NO CHANGE
Falling edge	L	INCREMENT by “one”

Function and Logical Diagrams

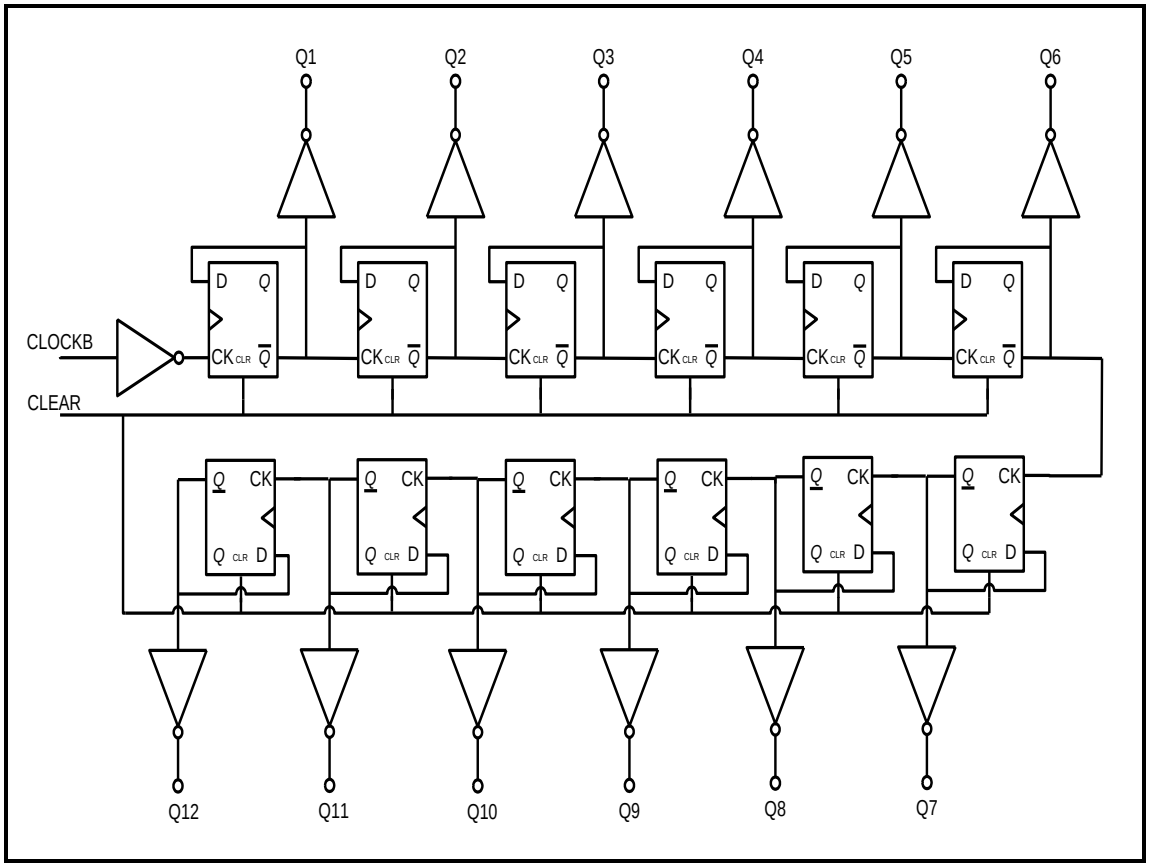


Figure 1. CHT-74-4040: simplified block diagram.

Absolute Maximum Ratings

Supply Voltage V_{DD} to GND	-0.5 to 5.5V
Voltage on any Pin to GND	-0.5 to V_{DD}+0.5V

ESD Rating

Human Body Model	Class 2

Operating Conditions

Supply Voltage V_{DD} to GND	3.3V to 5V (±10%)
Junction temperature	-55°C to +225°C
Voltage on any input pin	0V to VDD

DC Electrical Characteristics

Unless otherwise stated: T_j=25°C. **Bold** figures indicate values valid over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Supply voltage V_{DD}			5		V
Quiescent current I_{DD}	T_j=-55°C			30	nA
	T_j=225°C			**21**	µA
Minimum HIGH level output voltage V_{OH}	I_{OH}<4mA (source)	**4.67**	4.82		V
Maximum LOW level output voltage V_{OL}	I_{OL}<4mA (sink)		0.2	**0.4**	V
Minimum HIGH level input voltage V_{IH}		**3.7**	3.49		V
Maximum LOW level input voltage V_{IL}			2.16	**2**	V

Parameter	Condition	Min	Typ	Max	Units
Supply voltage V_{DD}			3.3		V
Quiescent current I_{DD}	T_j=-55°C			20	nA
	T_j=225°C			**21**	µA
Minimum HIGH level output voltage V_{OH}	I_{OH}<4mA (source)	**2.91**	3.03		V
Maximum LOW level output voltage V_{OL}	I_{OL}<4mA (sink)		0.28	**0.5**	V
Minimum HIGH level input voltage V_{IH}		**2.4**	2.1		V
Maximum LOW level input voltage V_{IL}			1.72	**1.5**	V

AC Electrical Characteristics

Unless otherwise stated: VDD=5V, T_j=25°C. **Bold** figures indicate values valid over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Temperature	Min	Typ	Max	Units
Output transition time t_{THL}, t_{TLH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	5.5	6.9	9	ns
		T_j=25°C	6.7	8.6	11.1	
		T_j=225°C	9.8	13.2	**18.2**	
Propagation delay time (Qn => Qn+1) t_{PHL}, t_{PLH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	2.3	3.3	4.7	ns
		T_j=25°C	3	4.4	6.32	
		T_j=225°C	4.8	7.3	**10.7**	
Propagation delay time (CLOCKB => Q1) t_{PHL}, t_{PLH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	11.6	15.7	21.7	ns
		T_j=25°C	14.2	19	27.5	
		T_j=225°C	20.8	29.7	**43**	
Propagation delay time (CLEAR => Qn) t_{PHL}, t_{PLH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	14.3	19.1	26	ns
		T_j=25°C	16.9	23.2	32.5	
		T_j=225°C	24.2	34.6	**49.6**	
Max clock frequency f_{MAX}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C		30.0		MHz
		T_j=25°C		23.8		
		T_j=225°C		**15.6**		
Minimum pulse width (CLOCKB) t_{WH}, t_{WL}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	12			ns
		T_j=25°C	18			
		T_j=225°C	**22**			
Minimum pulse width (CLEAR) t_{WH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	8			ns
		T_j=25°C	8			
		T_j=225°C	**12**			
Minimum setup time (CLEAR ⇔ CLOCK) t_S	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	6			ns
		T_j=25°C	7			
		T_j=225°C	**11**			

AC Electrical Characteristics

Unless otherwise stated: VDD=3.3V, T_j=25°C. **Bold** figures indicate values valid over the whole temperature range (-55°C < T_j < +225°C).

Parameter	Condition	Temperature	Min	Typ	Max	Units
Output transition time t_{THL}, t_{TLH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	8.8	12.7	19.5	ns
		T_j=25°C	10.7	16	24.3	
		T_j=225°C	15	22.6	**33.6**	
Propagation delay time (Qn => Qn+1) t_{PHL}, t_{PLH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	4.2	6.8	11.4	ns
		T_j=25°C	5.4	9	14.9	
		T_j=225°C	8	13	**21.4**	
Propagation delay time (CLOCKB => Q1) t_{PHL}, t_{PLH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	20.5	32	51.2	ns
		T_j=25°C	24.7	38.6	62.1	
		T_j=225°C	33.4	52.8	**84.2**	
Propagation delay time (CLEAR => Qn) t_{PHL}, t_{PLH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	25.6	39.3	62.5	ns
		T_j=25°C	30	46.4	74.2	
		T_j=225°C	39.6	62.3	**99.1**	
Max clock frequency f_{MAX}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C		14.2		MHz
		T_j=25°C		11.6		
		T_j=225°C		**8.5**		
Minimum pulse width (CLOCKB) t_{WH}, t_{WL}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	23			ns
		T_j=25°C	32			
		T_j=225°C	**40**			
Minimum pulse width (CLEAR) t_{WH}	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	16			ns
		T_j=25°C	21			
		T_j=225°C	**25**			
Minimum setup time (CLEAR ⇔ CLOCK) t_S	C_L=50pF, Input t_r=t_f= 6ns	T_j=-55°C	14			ns
		T_j=25°C	17			
		T_j=225°C	**22**			

AC Waveforms

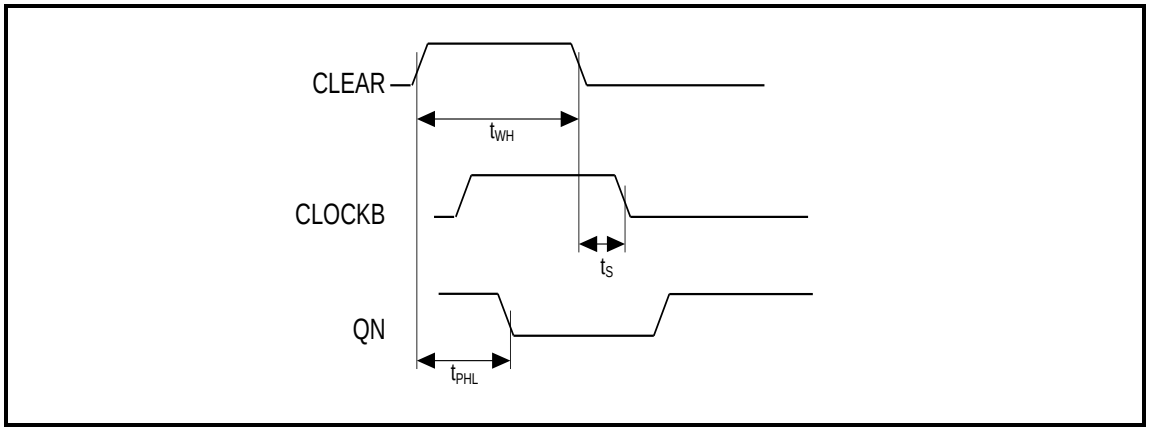


Figure 2. Waveform: minimum pulse width (CLEAR) and setup time (CLEAR to CLOCKB)

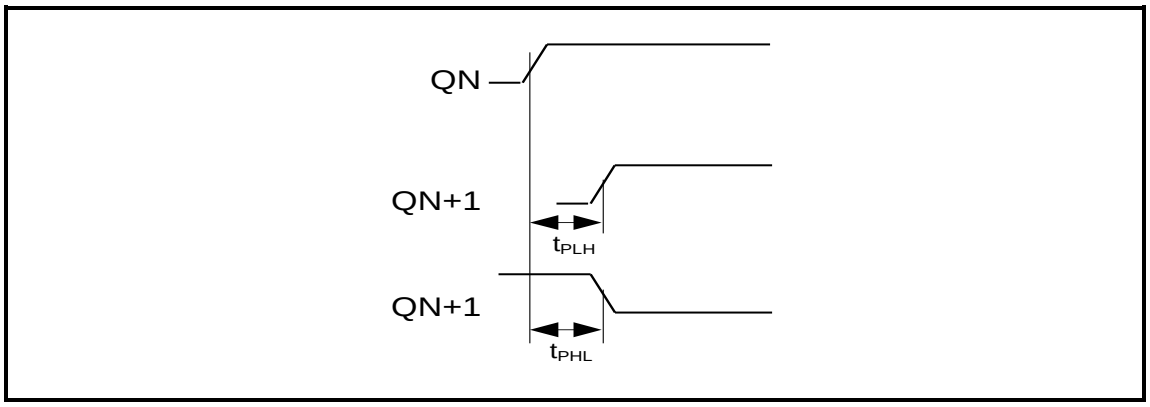


Figure 3. Wavefrom: propagation delay time

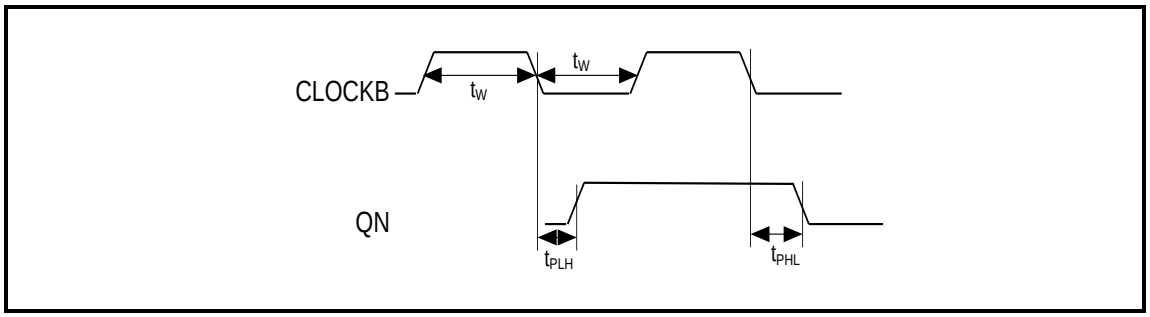
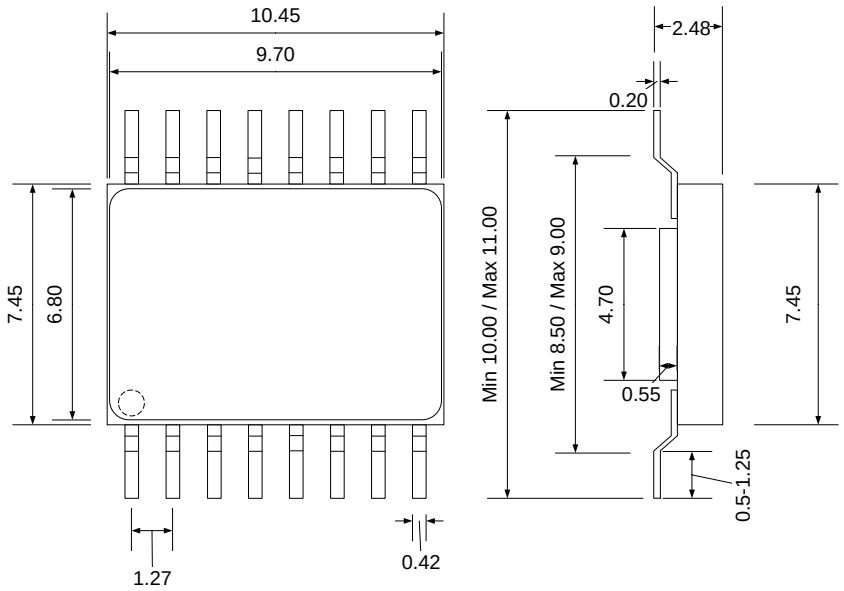


Figure 4: Waveform: propagation delay time, minimum pulse width (CLOCKB)

Ordering Information

Ordering Reference	Package	Temperature Range	Marking
CHT-744040A-CSOIC16-T	Ceramic SOIC16	-55°C to +225°C	CHT-744040A

Package Dimensions



Drawing CSOIC16 (mm +/- 10%)

Contact & Ordering

CISSOID S.A.

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