CHT-HYPERION DATASHEET

Revision: 1.9
23-Aug-21
(Last Modified Date)

High Temperature Half-Bridge Driver (high side and low side)

General Description

CHT-HYPERION is a high-side and low-side driver for power N-channel MOSFETs in DC-DC converters and electric motor control.

With typical on-resistances of 1Ω, both outputs can drive 1nF loads with 40ns propagation delays and 15ns transition times at 200°C. An adaptive non-overlap circuit reduces switching losses by preventing MOSFET's cross-conduction. The bootstrapped high-side floating driver can sustain voltage up to 50V.

An under-voltage lockout function holds the high-side switch off until the driver has sufficient voltage for proper operation. A crowbar input turns on the low-side driver independently of the input signal, and a low-side disable pin allows operation in non-synchronous mode. An OE pin enables the operation of both high- and low-side drivers.

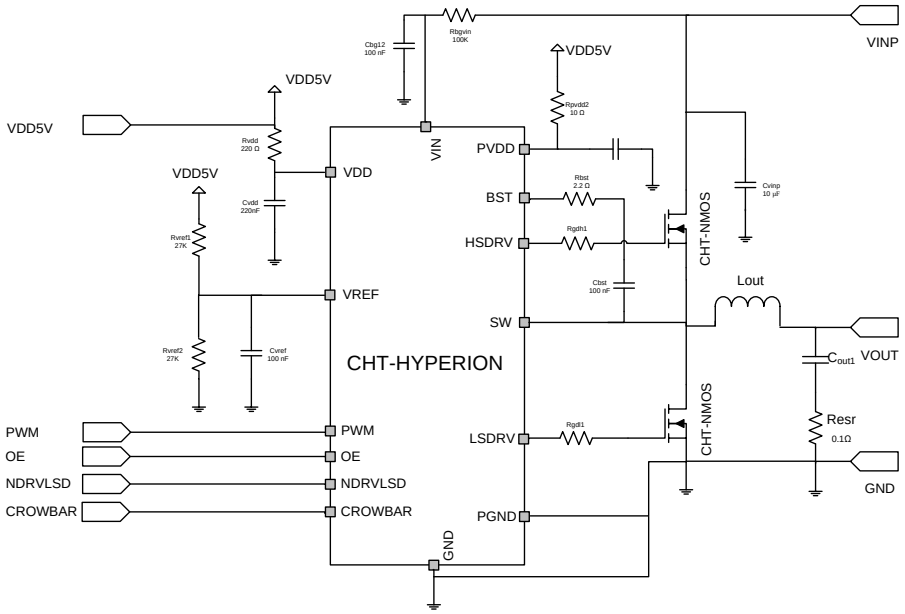
Features

- Fast rise and fall times
- Output peak current in excess of 1A
- Floating High-side driver sustain boost voltages of up to 50 V
- Integrated High-Side Bootstrap Diode
- All-in-one synchronous buck driver
- Adaptive non-overlap circuit
- Output enable control
- Low-side driver disabling
- Crowbar control
- Under voltage lockout (UVLO)
- Validated at 225°C for 43800 hours (CDIL28) and 20000 hours (CSOIC28) (and still on-going)
- Operational from -55°C to +225°C (Tj)

Applications

DC-DC Converters and Electric Motor Control for Oil&Gas, Industrial, Aerospace & Automotive

Typical Application



Recommendation

Due to high dV/dT & dI/dT in systems using Drivers, parasitic inductance on SW node can lead to voltage glitches on CHT-HYPERION pins (SW, HSDRV, LSDRV); this can cause a potential violation of the absolute maximum ratings. This situation is particularly critical at system start-up when using high duty cycle.

Cissoid recommends to

1. put a 50Ω resistance (Rgdh1, Rgdl1) on both HSDRV and LSDRV pins
2. perform the system start-up with low duty cycle
3. first test the application in open-loop to check that none of the nodes exceed the absolute maximum ratings

Functional Block Diagram

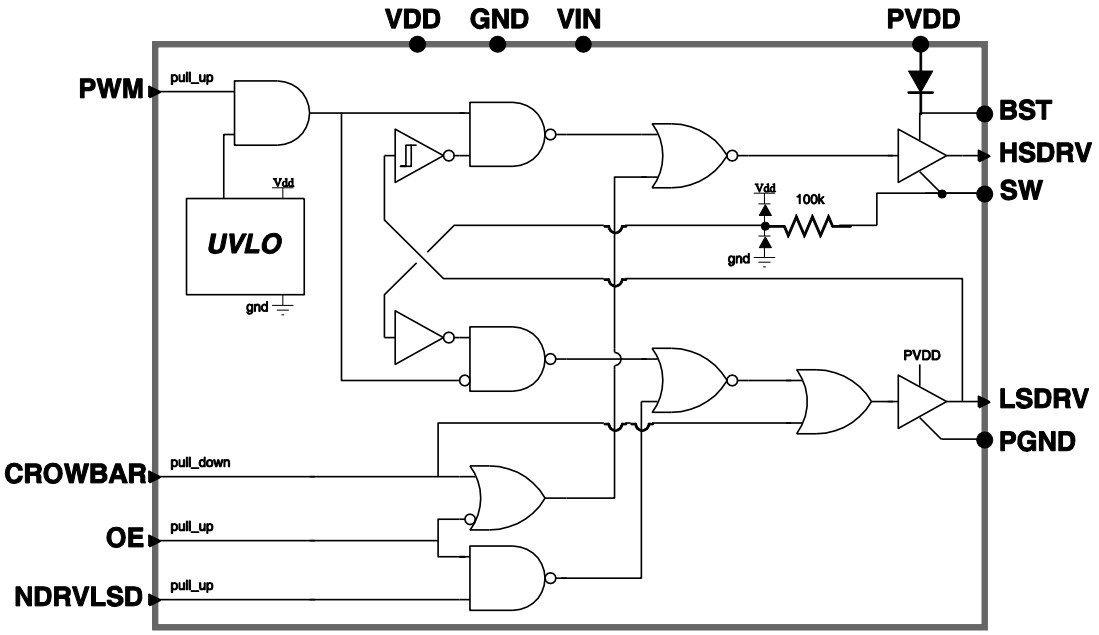
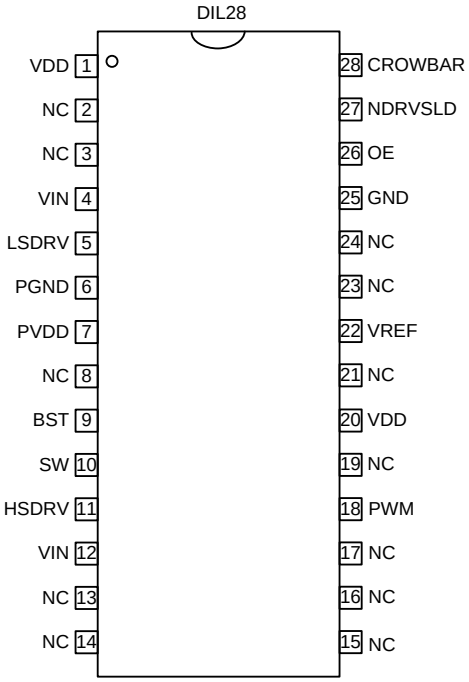


Table 1. Truth table.

CROWBAR	OE	NDRVLSD	ULVO	High-side Driver	Low-side Driver
0	1	**1**	**$V_{DD} < V_{thUVLO}$**	OFF	ON
0	1	**0**	**$V_{DD} < V_{thUVLO}$**	OFF	OFF
1	X	X	X	OFF	ON
0	**0**	X	X	OFF	OFF
0	1	**0**	$V_{DD} > V_{thUVLO}$	PWM	OFF
0	1	1	$V_{DD} > V_{thUVLO}$	PWM	/PWM

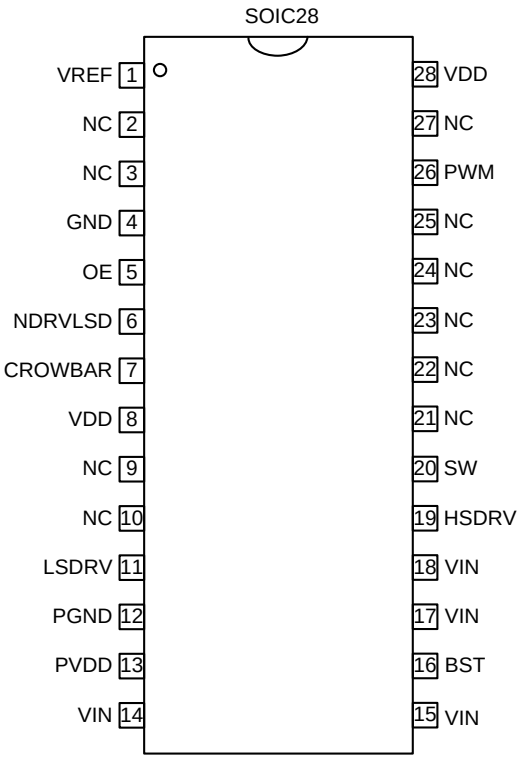
Package Configurations: CDIL28



Pin Description

Pin #	Pin Name	Pin Description
1	VDD	Connect to an external 5V supply.
2	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
3	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
4	VIN	Connect to a filtered VINP (see Typical Application section).
5	LSDRV	Low side driver output (0/5V vs. Power ground).
6	PGND	Power ground of output driver. Connect to ground.
7	PVDD	Power supply of output driver. Connect to an external 5V supply.
8	NC	Not connected.
9	BST	Bootstrap supply input for the high-side driver. Connect to the bootstrap capacitor top node.
10	SW	Switching input node. This is the bottom node of the high-side driver. Connect it to the bootstrap capacitor bottom node. SW node is also used as an internal feedback for the non-overlap control.
11	HSDRV	Floating output (0/5V vs. SW node) of the high side driver.
12	VIN	Connect to a filtered VINP (see Typical Application section).
13	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
14	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
15	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
16	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
17	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
18	PWM	Driver input (0/5V) from an external controller.
19	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
20	VDD	Connect to an external 5V supply.
21	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
22	VREF	Use for internal control. It is mandatory to Connect a resistive divider (27kΩ) between VDD, Vref and GND pins in order to generate a 2.5V threshold on this Vref pin
23	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
24	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
25	GND	Connect to ground.
26	OE	Active high Output Enable. Internally pulled-up. See truth table below.
27	NDRVLSD	Active low Driver Low Side Shut Down. When driven low, the Low Side driver is turned OFF (output low). Internally pulled-up. See truth table below.
28	CROWBAR	When driven high, it turns ON the low side driver and turns OFF the high-side driver, whatever the “OE”, “NDRVLSD” and “PWM” state. Internally pulled-down. See truth table below.

Package Configurations: CSOIC28



Pin Description

Pin #	Pin Name	Pin Description
1	VREF	Use for internal control. It is mandatory to Connect a resistive divider (27kΩ) between VDD, Vref and GND pins in order to generate a 2.5V threshold on this Vref pin
2	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
3	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
4	GND	Connect to ground.
5	OE	Active high Output Enable. Internally pulled-up. See truth table below.
6	NDRVLSD	Active low Driver Low Side Shut Down. When driven low, the Low Side driver is turned OFF (output low). Internally pulled-up. See truth table below.
7	CROWBAR	When driven high, it turns ON the low side driver and turns OFF the high-side driver, whatever the “OE”, “NDRVLSD” and “PWM” state. Internally pulled-down. See truth table below.
8	VDD	Connect to an external 5V supply.
9	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
10	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
11	LSDRV	Low side driver output (0/5V vs. Power ground).
12	PGND	Power ground of output driver. Connect to ground.
13	PVDD	Power supply of output driver. Connect to an external 5V supply.
14	VIN	Connect to a filtered VINP (see Typical Application section).
15	VIN	Connect to a filtered VINP (see Typical Application section).
16	BST	Bootstrap supply input for the high-side driver. Connect to the bootstrap capacitor top node.
17	VIN	Connect to a filtered VINP (see Typical Application section).
18	VIN	Connect to a filtered VINP (see Typical Application section).
19	HSDRV	Floating output (0/5V vs. SW node) of the high side driver.
20	SW	Switching input node. This is the bottom node of the high-side driver. Connect it to the bootstrap capacitor bottom node. SW node is also used as an internal feedback for the non-overlap control.
21	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
22	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
23	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
24	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
25	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
26	PWM	Driver input (0/5V) from an external controller.
27	NC	Not connected internally; can be left floating or connected to any net to ease PCB routing
28	VDD	Connect to an external 5V supply.

Absolute Maximum Ratings

Devices stressed above these absolute maximum ratings could present permanent damage. Exposure to any of these maximum ratings repeatedly or for extended periods may permanently affect the device reliability. These ratings are considered individually (not in combination). If not specified, voltages are related to the power ground PGND.

Parameter	Min.	Max.	Units
VDD	0	5.5	V
VIN	0	52	V
PWM, OE,NDRVLSD,CROWBAR	0	"VDD"+0.5	V
SW	-2 (continuous) -TBD(transient)	52	V
BST (vs. "SW")	0	5.5	V
HSDRV	"SW"-1	"BST"+0.5	V
LSDRV	0 (continuous) TBD(transient)	"VDD"+0.5	V
GND	-0.5	0.5	V
PVDD	"VDD"-1	"VDD"+1	V
Junction Temperature		250	°C
ESD Rating (Human Body Model)	1 (expected)		kV

With high voltage/high frequency switching, parasitic inductors and capacitors can create current and voltage glitches beyond the absolute maximum rating of CHT-HYPERION. In order to prevent exceeding absolute maximum ratings, it is recommended to take special care to minimize parasitics at PCB level on all high voltage nodes.

Electrical Characteristics

Unless otherwise stated: V_{DD}=5V, T_j=25°C. **Bold underlined** values indicate values over the whole operational temperature range (-55°C < Tj < +225°C).

Parameter	Condition	Min	Typ	Max	Units
Input Supply					
Power supply[1] (PVDD)		**4.5**		**5.5**	V
V_{DD}		**4.5**		**5.5**	V
VIN[1]		**4.0**		**50**	V
I(VDD)[2]	200kHz, with serial RC load of 1nF; 5Ω		3.45		mA
Digital Input Controls (PWM; OE; NDRVLSD; CROWBAR)[3]					
OE, NDRVLSD, PWM	Internal pull-up current	**25**		**85**	µA
CROWBAR	Internal pull-down current	**18**		**60**	µA
Input High		**3.7**		**VDD+0.3**	
Input Low		**-0.3**		**2**	
High-Side Driver					
Output sourcing resistance[4]	Tj=225°C; V(SW)=0; V(BST)=5V		1.5		Ω
Output sinking resistance4	Tj=225°C; V(SW)=0; V(BST)=5V		1.64		Ω
Leakage path from SW[5]	Ta=200°C		100		µA
Transition times and propagation delays[6]	Ta=200°C Serial RC load: 1nF; 5Ω				
tpdh			40		ns
tpdl			84		ns
Rise Time (tr) (10%-90%)			15		ns
Fall Time (tf) (90%-10%)			14		ns
Low-Side Driver					
Output sourcing resistance (PMOS) 4	Ta=225°C ; V(SW)=0 ; V(BST)=5V		1.5		Ω
Output sinking resistance4 (NMOS) 4	Ta=225°C ; V(SW)=0 ; V(BST)=5V		1.64		Ω
Transition times and propagation delay6	Ta=200°C Serial RC load: 1nF; 5Ω				
tpdh			43		ns
tpdl			39		ns
Rise Time (tr) (10%-90%)			17		ns
Fall Time (tf) (90%-10%)			15		ns
Under Voltage LockOut (UVLO)					
UVLO Threshold Voltage[7] (V_{thUVLO})	220Ω in series for all VDD (except on PVDD)				
	Ta=-55°C		4.3		V
	Ta=25°C		3.9		V
	Ta=125°C		3.4		V
	Tj=225°C		2.9		V
Bootstrap Diode					
Forward current[8]	Ta=200°C ; $V_{forward}$=1.4V		875		mA
Reverse current	Ta=200°C ; $V_{reverse}$=30V			5	µA
Reverse breakdown		**50**			V

1 See Typical Application section.
2 See Figure 2.
3 Internally pulled up or down. They may be left floating if they are not used. (See the “Pin Description” section).
4 See Figure 3
5 See the resistive leakage path of SW node on the section “Functional Block Diagram”.
6 See Figure 1. The timing is defined on the 1nF load, after a 5Ω serial resistor.
7 Above this threshold, the drivers are correctly operating. Bellow this threshold, the high-side is turned off and the low side is turned on. The typical threshold dependence on temperature is VthUVLO=4.01V-0.005*Temp(°C).
8 See Figure 4.

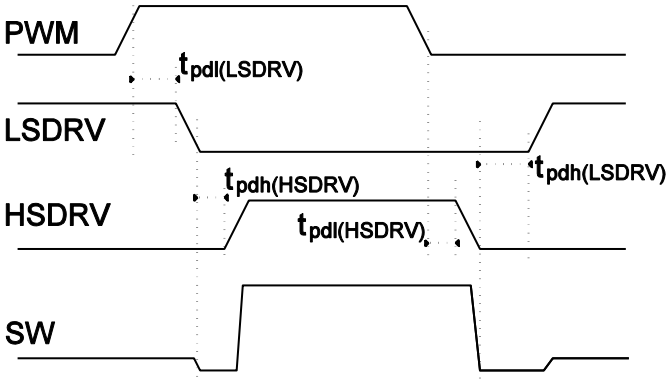


Figure 1: Driver timing diagram

Typical Performance Characteristics

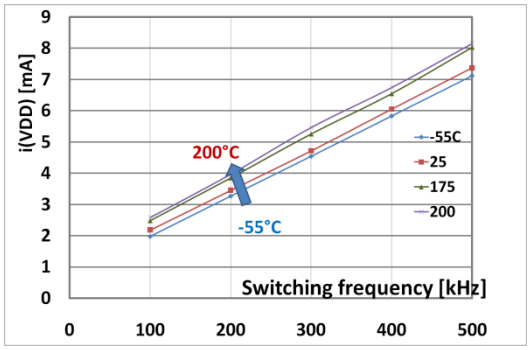


Figure 2: Driver current consumption vs. Frequency and Temperature. C_L=1nF; R_S=5Ω

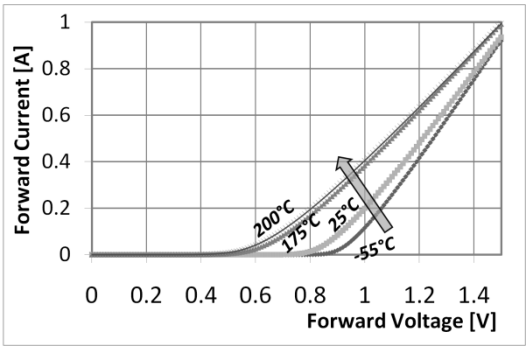


Figure 4: Bootstrap diode forward current over ambient temperature

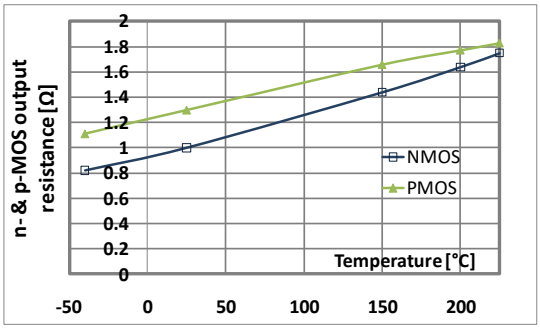


Figure 3: Driver output resistance over temperature

General Description

The CHT-HYPERION circuit is a dual n-MOSFET driver (5V). It is optimized for driving a synchronous buck converter topology. The high side driver output follows the PWM logic input while the low side driver presents a complementary control. A feedback from the low-side gate and from the SW switching node ensures a non-overlap delay between the low-side and high-side controls.

Each driver is able to drive a load capacitance of 3nF at speeds up to 500kHz.
The circuit includes an Under Voltage Lockout block which turns off the high-side driver at low supply (VDD) voltages.

High-Side Driver (HSDRV) and associated Bootstrap

The HSDRV is designed to drive an external floating power n-MOSFET with a 5V logic level. A bootstrap capacitor C_{boots} of 100nF between "BST" and "SW" nodes ensures the correct supply of the driver whatever the "SW" node voltage (see the electrical specifications table). A high logic level on the "PWM" input gives (after some propagation delay) a high level at the high-side driver output. Note that the HSDRV output cannot remain high for long time as it takes its energy from C_{boots}. This means that the driver cannot accept a 100% duty-cycle at its PWM input (except if the "SW" node is tight to ground). The bootstrap capacitor is refilled through an integrated bootstrap diode (Figure 4) when the "SW" node goes below PVDD (thanks to an external inductive load or thanks to the turn on of the low-side). The BST, HSDRV and SW nodes are all floating nodes with respect to all other pins of the circuit (except a 100kΩ resistive path to ground from the SW node. See the "Functional Block Diagram"). In order to reduce the driver output transient slopes and HF spikes, it is recommended to add an external resistor of some tens of ohms between the driver output and the external power n-MOSFET gate. Without such resistor, excessive HF spikes may damage the driver.

In order to implement a non-overlap control between outputs of the low- and the high-side driver, the circuit checks that the output of the LS driver is below a threshold of about 2.5V (with a hysteresis on the threshold of about 1V) before allowing the turn on of the HS driver.

Bootstrap capacitance sizing

Since the High-Side driver of CHT-Hyperion does not include a charge pump feature and since this driver has a static current consumption of 100 µA (at 225°C), the bootstrap capacitance will gradually get discharged when this driver is ON.

The maximum on-time of the High-Side driver can be expressed as follows:

- Ton = Cbst * 0.5V/100 µA

Where Cbst is the value of the bootstrap capacitance and "0.5V" is the max acceptable voltage drop (to maintain proper operation of this driver) on this bootstrap capacitance wrt to the maximum recharged level (5V).
With a bootstrap capacitance of 100nF, this leads to a maximum on-time of 500µs.

If the application requires longer on-time, either bootstrap capacitance value can be increased or system can force a regular short turn-on of the Low-Side driver to recharge the bootstrap capacitance.

Low-Side Driver (LSDRV)

The LSDRV is designed to drive an external power n-MOSFET with 5V logic level. This driver output is referred to the (power) ground. During the transients, large peak current can occur across PVDD and PGND nodes.
In order to implement a non-overlapping between the low- and the high-side driver output, the circuit checks that the switching node "SW" voltage is below a threshold of about 2.5V before allowing the turn on of the LS driver. As the "SW" node can rise up to 50V, the non-overlap feedback is internally clamped between ground and VDD using two internal diodes and a serial of 100k-ohms.

Under Voltage Lockout

An integrated under voltage lockout is implemented with a threshold on the VDD supply between 2.5V and 4.5V (depending on temperature). If the supply is lower than the threshold, the HSDRV output is pulled down while the LSDRV is pulled up to VDD. Note that ENDR, NDRVLSD & CROWBAR input have priority with respect to the under voltage lockout block. In all cases, the HSDRV is low when the under voltage condition is activated. When VDD is close to the UVLO threshold, the UVLO output can present an unknown logic level (i.e. the HSDRV output can be zero or follow the PWM input). In order to reduce the VDD range for which the state of the UVLO flag is unknown, it is recommended to use a 220Ω resistor between the external 5V supply and all “VDD” pins (except the PVDD pin). This increases the UVLO threshold by about 100mV.

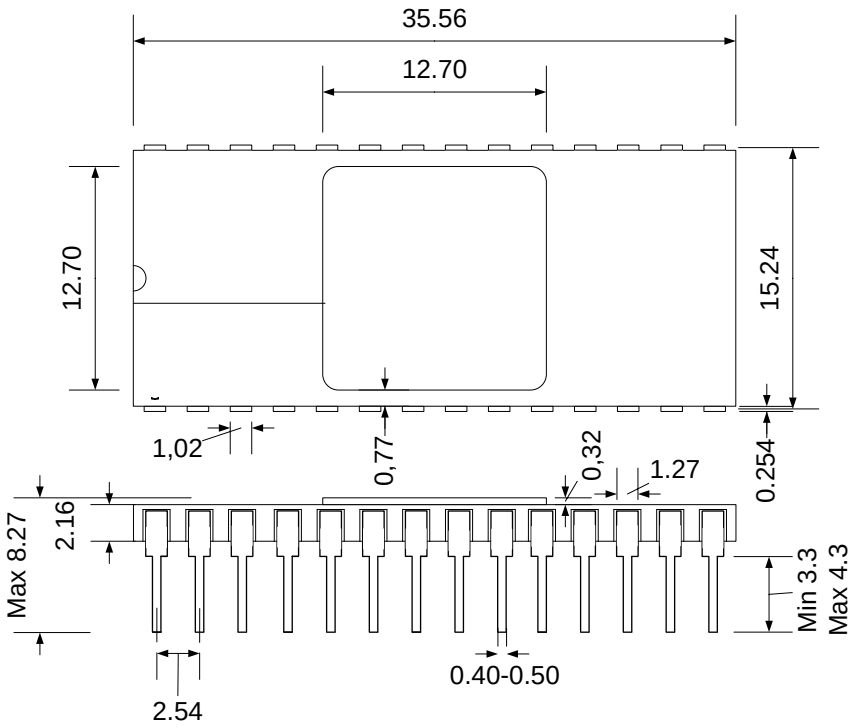
Application development

Cissoid recommends that in the application testing process, the power supply is gradually increased starting from 7V; at each step, presence of glitches should be checked. If any and if those glitches are close to the maximum absolute maximum ratings, the application should be reworked to decrease drastically the amplitude of those glitches.
Be aware as well that when using Hyperion in a loop, any loop instability can lead to signals exceeding absolute maximum rating values.

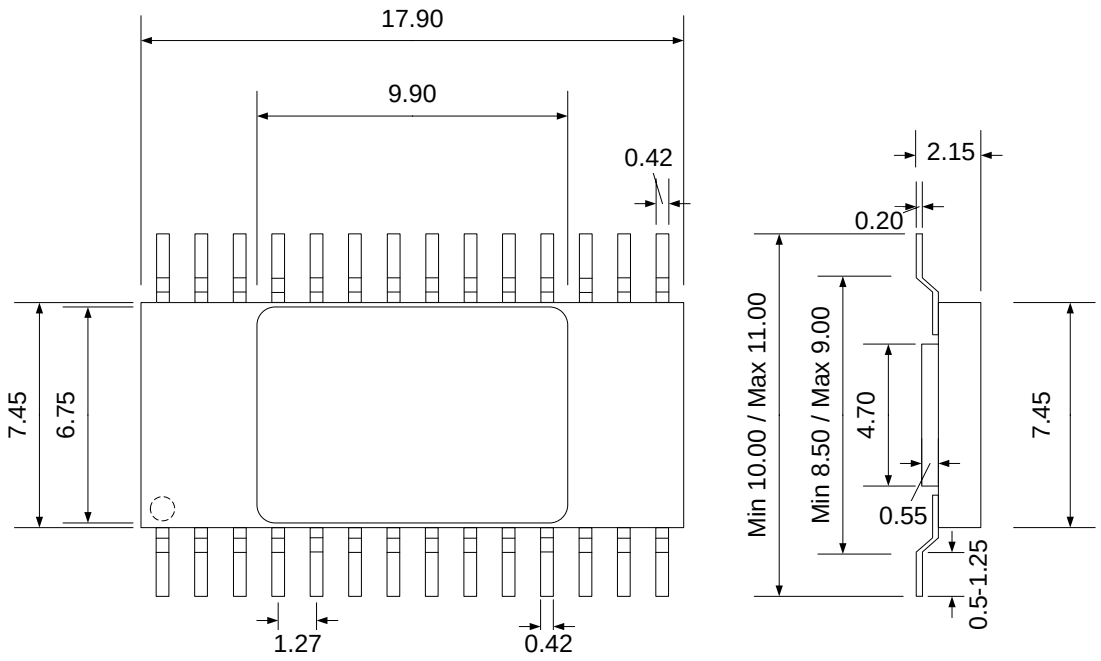
Ordering Information

Ordering Reference	Package	Temperature Range	Marking	Status
CHT-HYPERION-CDIL28-T	Ceramic DIL28	-55°C to +225°C	CHT-HYPERION	Not for new design
CHT-HYPERION-CSOIC28-T	Ceramic SOIC28	-55°C to +225°C	CHT-HYPERION	

Package Dimensions



Drawing CDIL28 (mm +/- 10%)



Drawing CSOIC28 (mm +/- 10%)

Contact & Ordering

CISSOID S.A.

Headquarters and contact EMEA:	CISSOID S.A. – Rue Francqui, 3 – 1435 Mont Saint Guibert - Belgium T : +32 10 48 92 10 - F: +32 10 88 98 75 Email: sales@cissoid.com
Sales Representatives:	Visit our website: http://www.cissoid.com

Disclaimer

Neither CISSOID, nor any of its directors, employees or affiliates make any representations or extend any warranties of any kind, either express or implied, including but not limited to warranties of merchantability, fitness for a particular purpose, and the absence of latent or other defects, whether or not discoverable. In no event shall CISSOID, its directors, employees and affiliates be liable for direct, indirect, special, incidental or consequential damages of any kind arising out of the use of its circuits and their documentation, even if they have been advised of the possibility of such a damage. The circuits are provided "as is". CISSOID has no obligation to provide maintenance, support, updates, or modifications.

CISSOID has the right to change, adapt or modify this document without any prior notice. Please contact CISSOID to get the last up to date information.